

A CCD Vertex Detector for the Future e^+e^- Linear Collider

LCWS 2000



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on behalf of the LCFI Collaboration

<http://hep.ph.liv.ac.uk/~green/lcfi/home.html>

Ideas based on SLD vertex detector (307 M Pixels), extended to 799 M pixels.

- Physics goals
- Detector design overview
- Layer thickness
- Readout rate; CCD architecture

Physics Goals

- TeV regime may be characterised by a wide range of SM and beyond-SM processes, typically with small cross-sections, many with high multiplicities of heavy-quark jets, eg

$e^+e^- \rightarrow t\bar{t}$ usually 6 jets, two b -flavoured and two c -flavoured

$e^+e^- \rightarrow t\bar{t}h$ usually 8 jets, four b -flavoured

$e^+e^- \rightarrow AH$ 12 jets, four b -flavoured

- Precision measurements (eg of Higgs branching ratios) can distinguish between SM and other models.

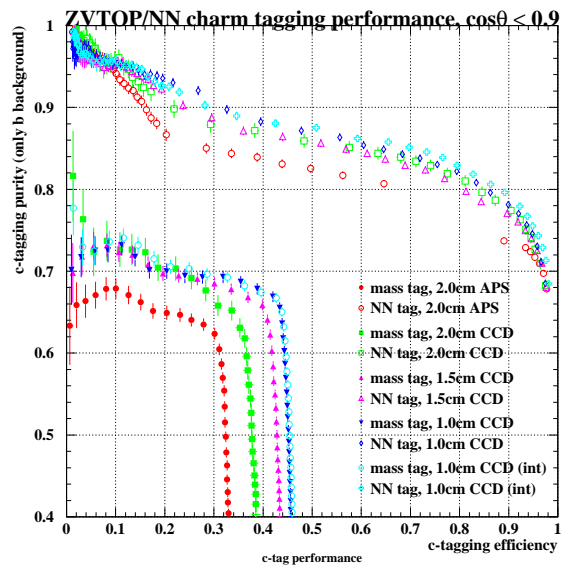
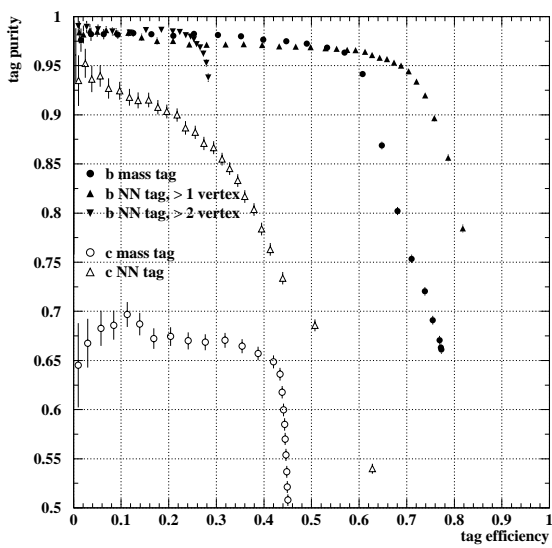
→ Thus, need for highly efficient and pure b and c tags is evident

- Vertex charge is valuable to distinguish b from \bar{b} and c from \bar{c}

Important for angular analyses eg for

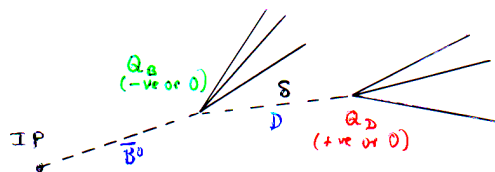
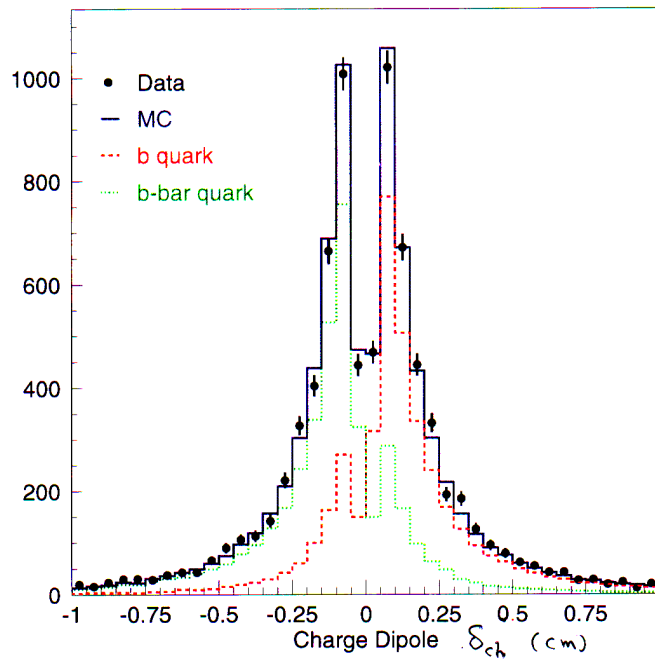
ZZH and $Z\gamma H$ anomalous couplings

- Charge dipole (demonstrated in SLD) can distinguish b from \bar{b} even in case of B^0 final state



$$\delta_{ch} = \frac{Q_b - Q_c}{|Q_b - Q_c|} \cdot \delta$$

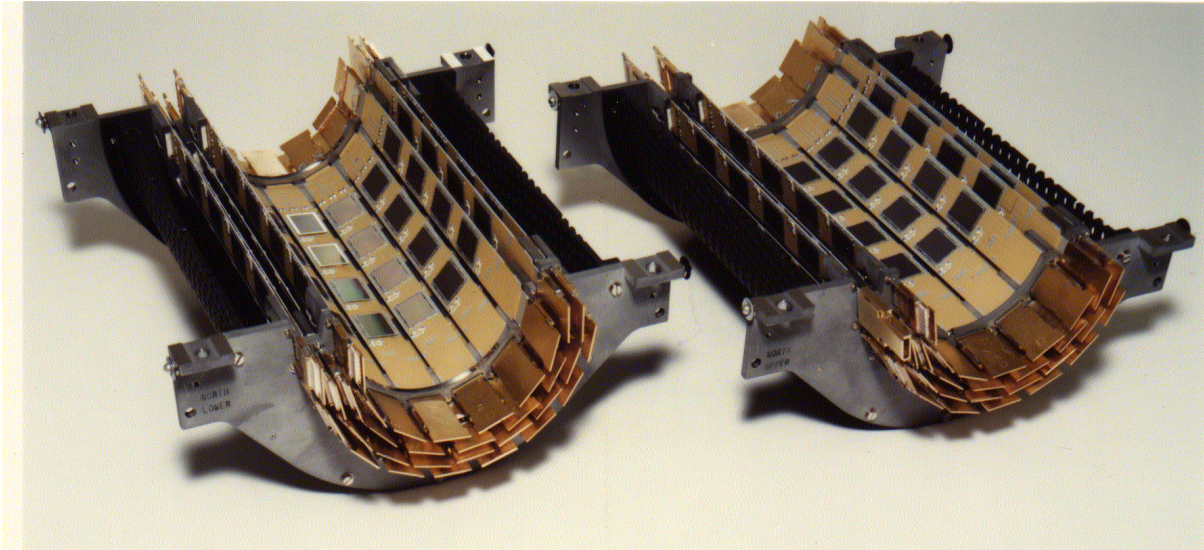
SLD Preliminary



The SLD Vertex Detectors

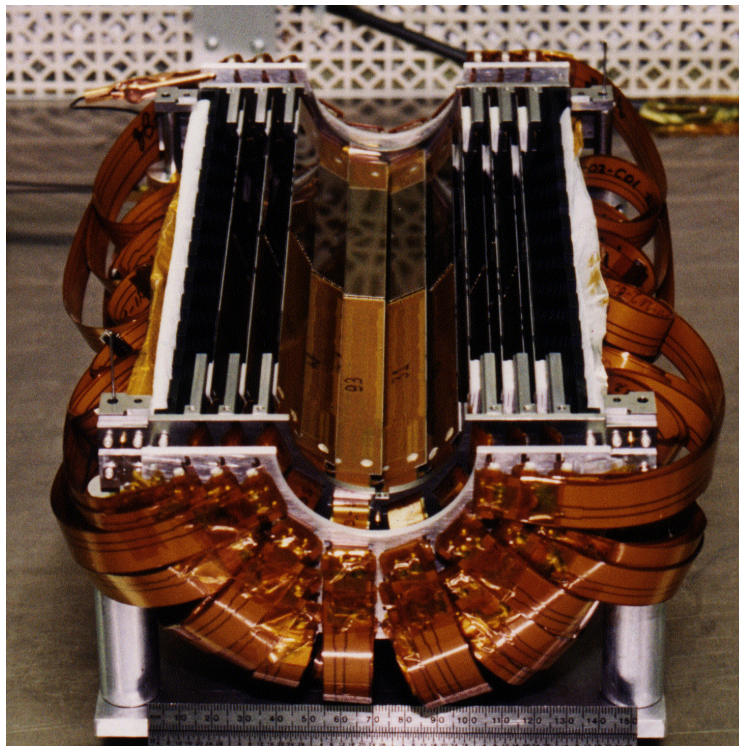
VXD2

Proc 26th Int Conf on HEP, Dallas TX (1992)

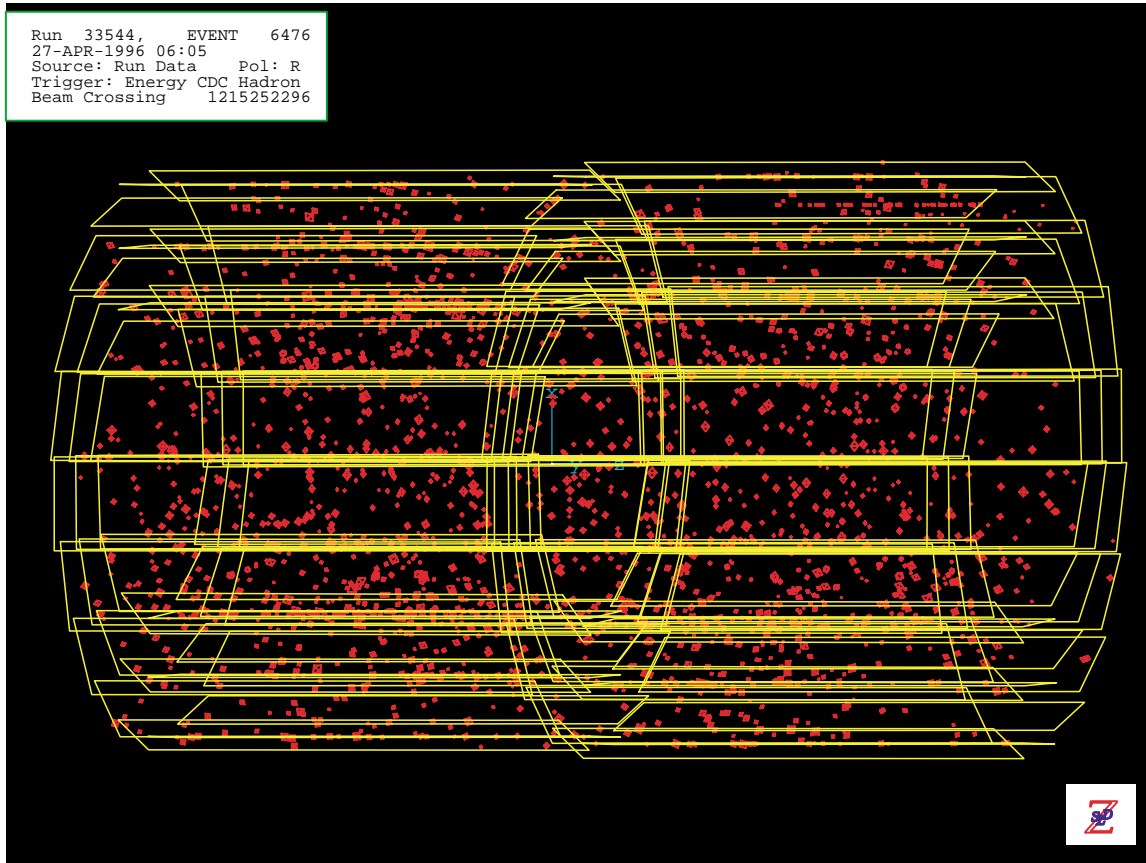


VXD3

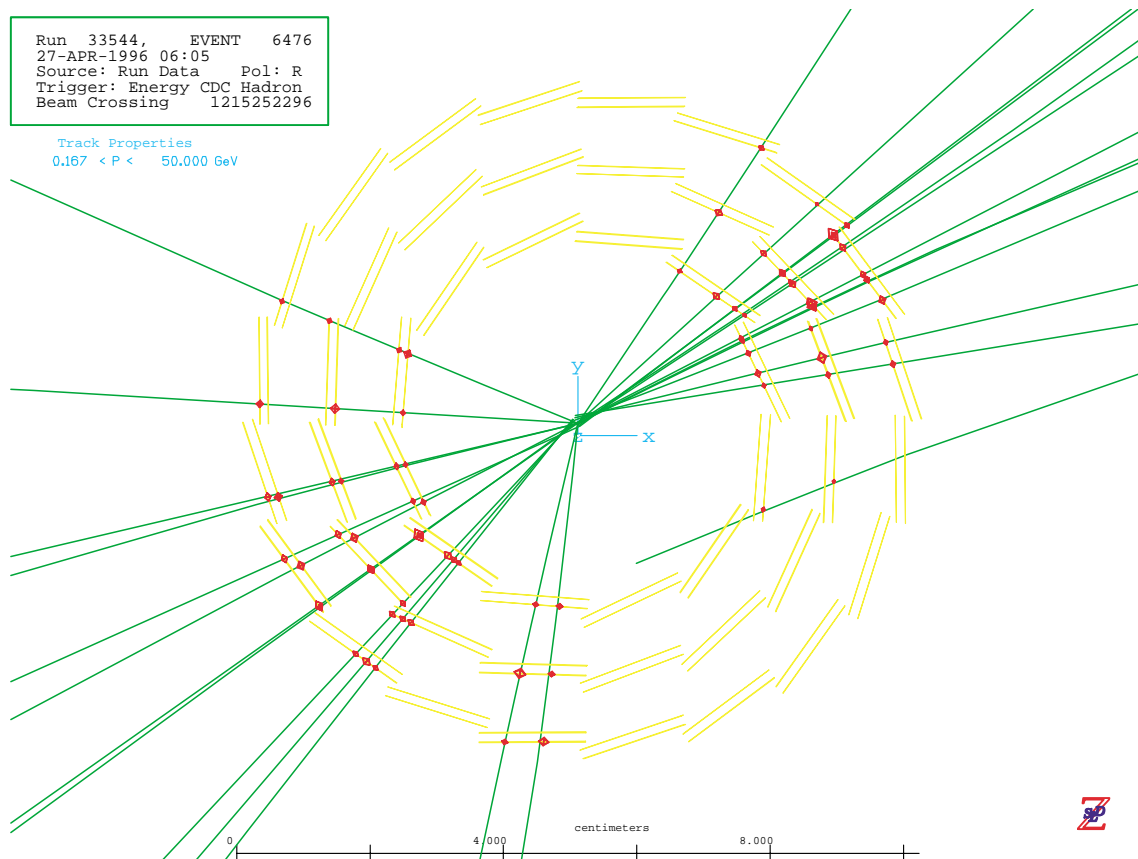
NIM A400 (1997) 287



e^+e^- linear collider will inevitably have high background at small radii

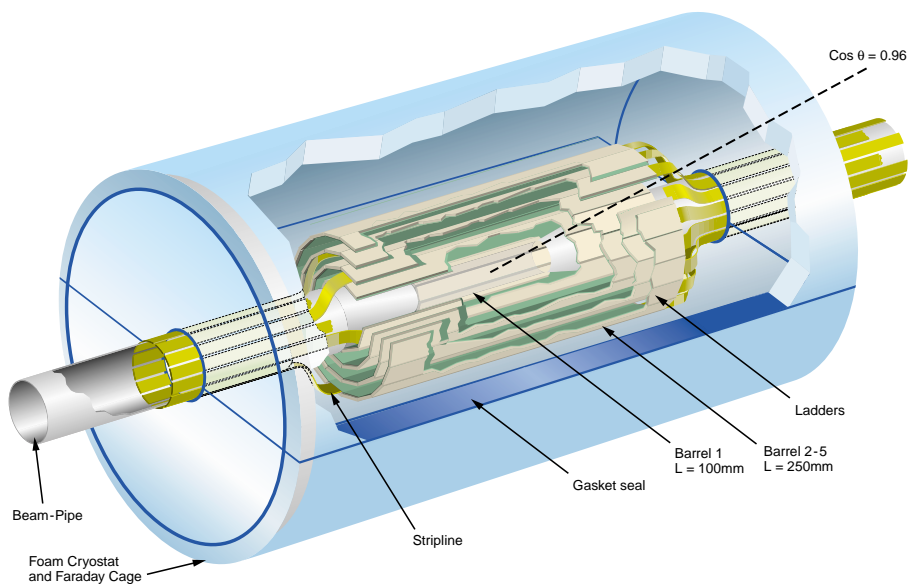
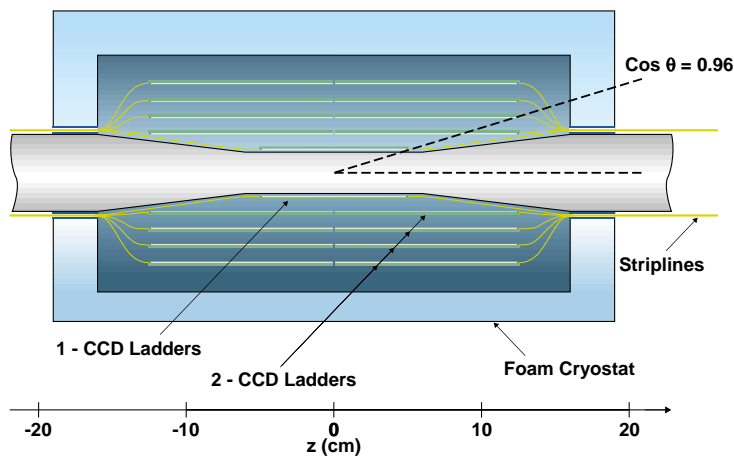


A pixel detector is extremely tolerant of this background



The future LC vertex detector

- Studies of the Linear Collider Flavour ID collaboration (LCFI)
- Detailed studies in context of TESLA detector:
 - $R_{bp} = 14$ mm and 4 Tesla solenoid
 - L1 active length 10 cm
 - 3-hit coverage to $\cos\theta = 0.96$

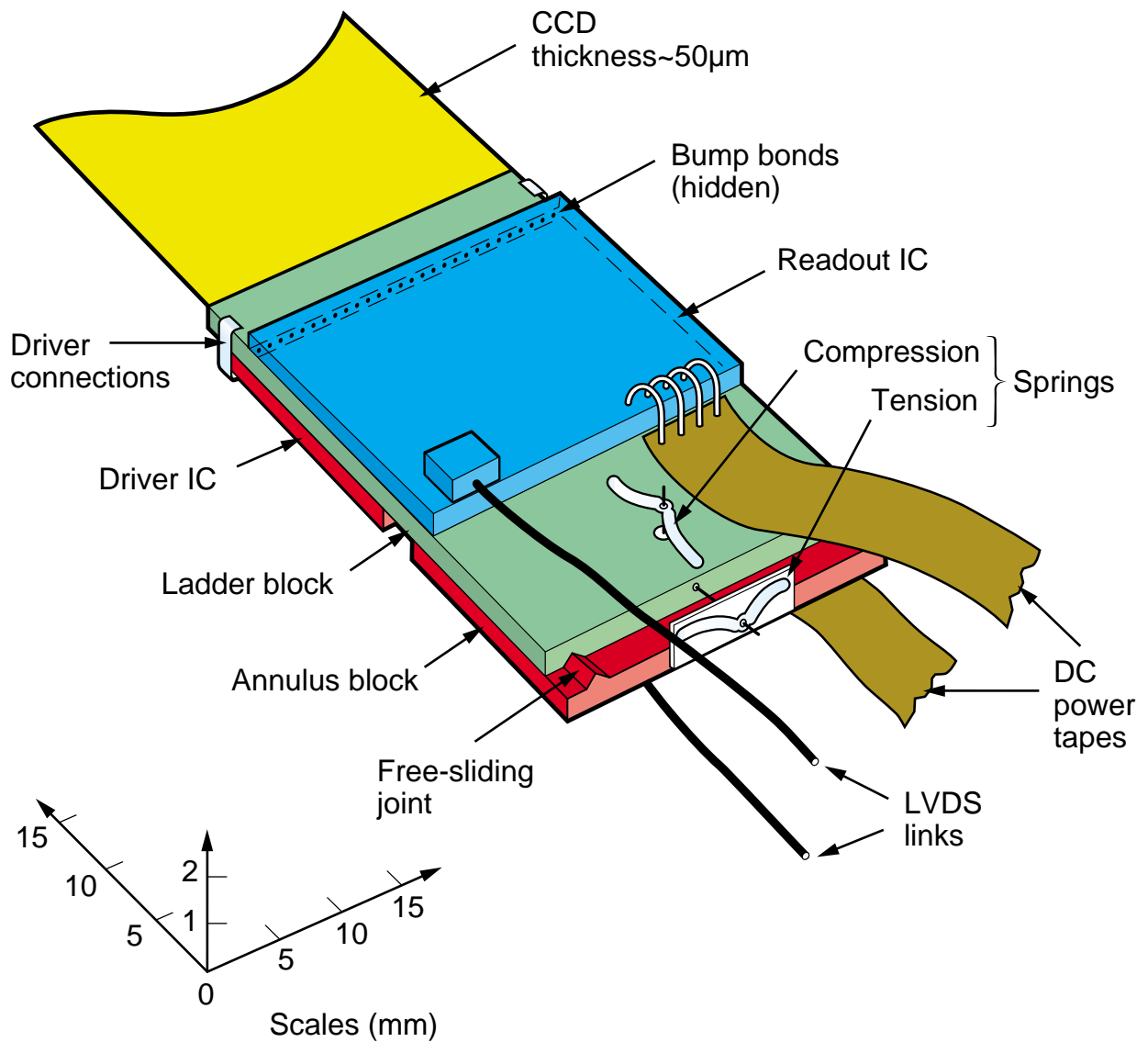


SLD & Future LC Detector Properties

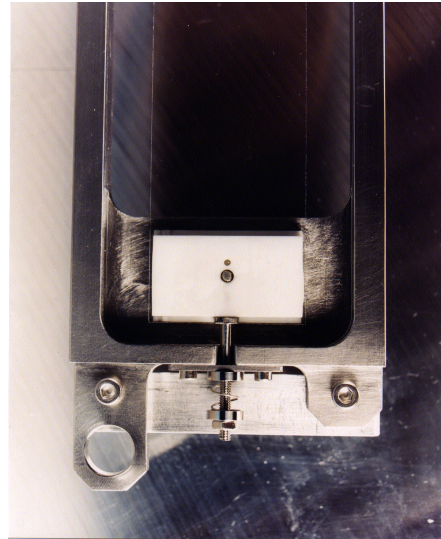
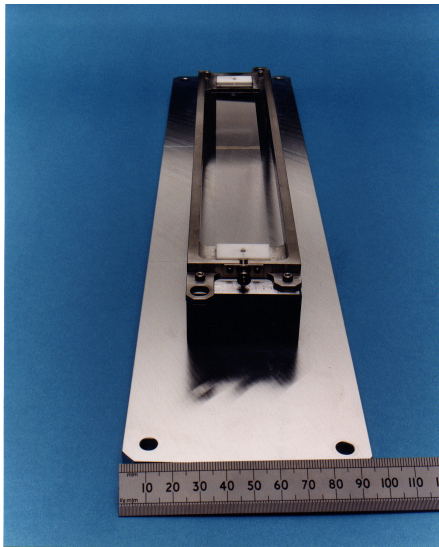
Detector	VXD2	VXD3	Future LC
CCDs	480	96	120
CCD active area (cm ²)	1.2	12.8	27.5
Number of pixels ($\times 10^6$)	120	307	799
Effective no. of layers	2	3	5
Inner layer radius (mm)	28	28	15
Layer thickness (% X_0)	1.1	0.4	0.06
$(\cos \theta)_{\max}$ (2-hit)	0.75	0.90	0.96
Imp. param resoln. $\sigma_{r\phi}$	$11 \oplus 70 / p \sin^{3/2} \theta$	$9 \oplus 33 / p \sin^{3/2} \theta$	$3.5 \oplus 6.5 / p \sin^{3/2} \theta$
σ_{rz}	$38 \oplus 70 / p \sin^{3/2} \theta$	$17 \oplus 33 / p \sin^{3/2} \theta$	$3.5 \oplus 6.5 / p \sin^{3/2} \theta$
Readout time	160 ms	216 ms	50/250 μ s (8 ms for NLC)

Layer Thickness

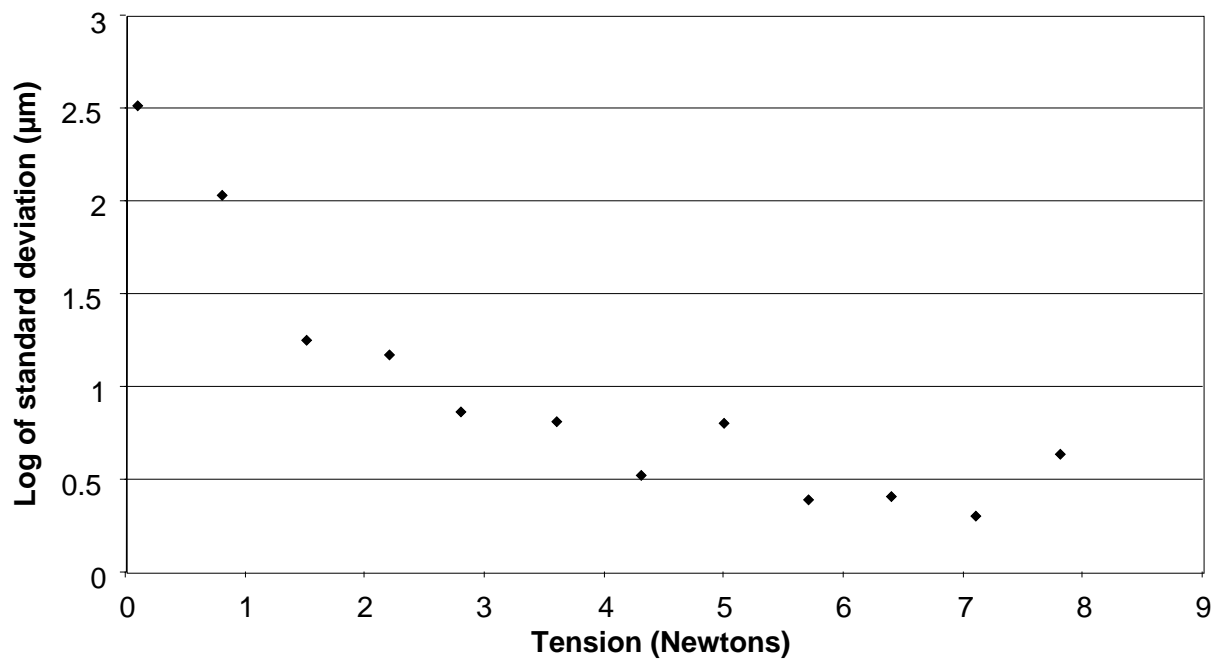
- Currently pushing the 'unsupported silicon' option



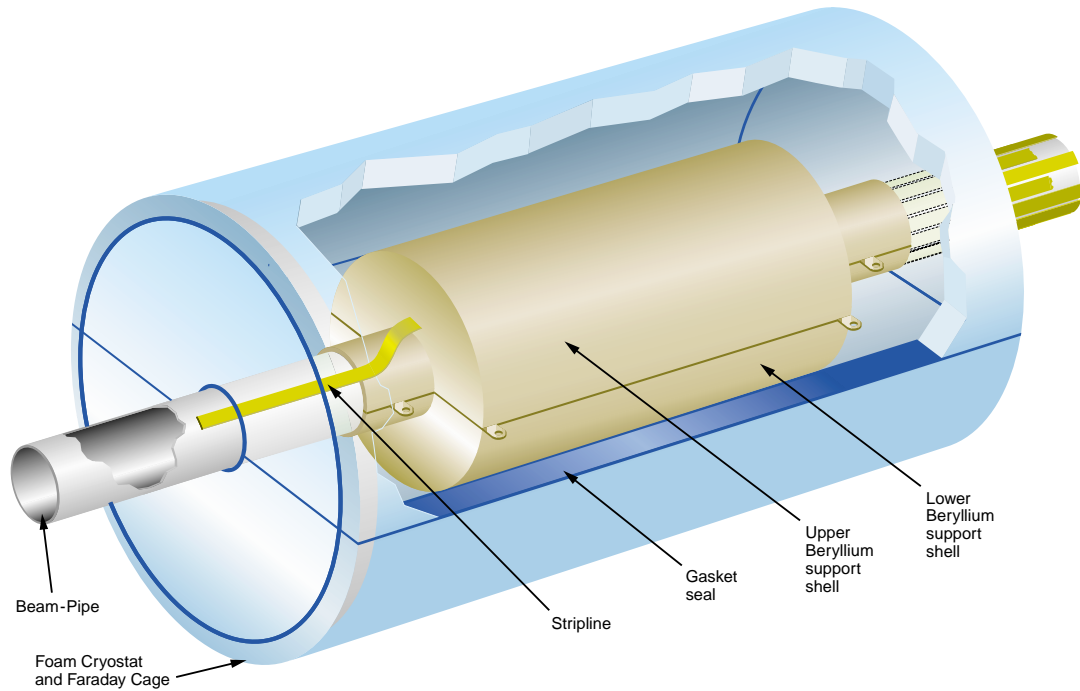
- Results with thin glass CCD models are most encouraging



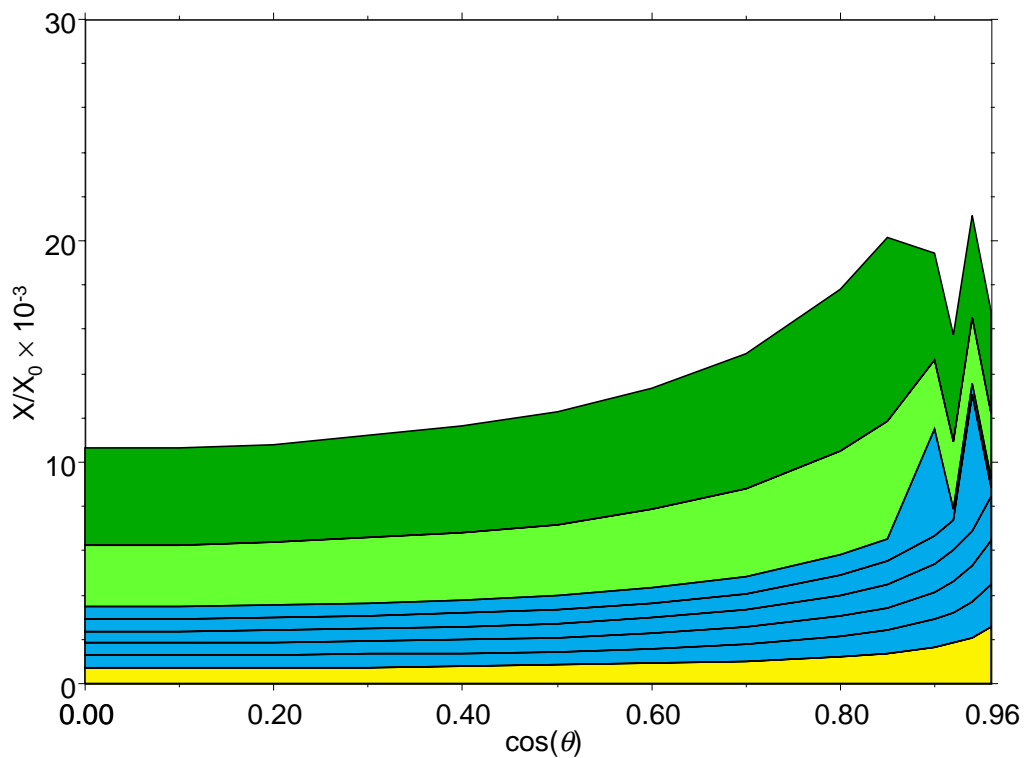
- Assisted by the strong technology evolving for PTPs (paper-thin packages)



0.06% X_0 /layer would be excellent, but this imposes pressure on the beampipe thickness



- 0.07% X_0 may be possible (0.25 mm beryllium), by using the VXD support shell for strain relief



- Layer 1-3 provide first class coverage to $\cos \theta = 0.96$
- < 1% X_0 total

Readout Rate/CCD Architecture

NLC: $190 \times 120 = 22.8 \times 10^3$ bunches/s

TESLA: $2820 \times 5 = 14.1 \times 10^3$ bunches/s

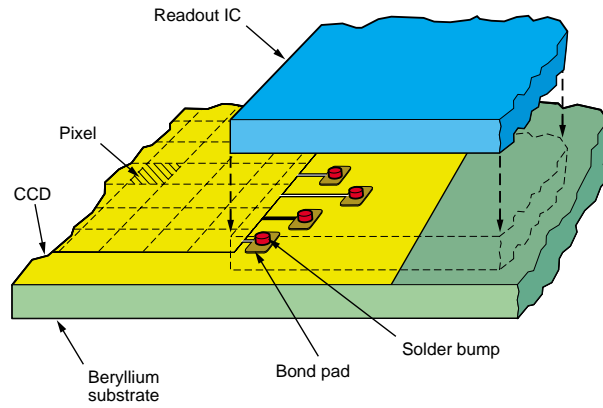
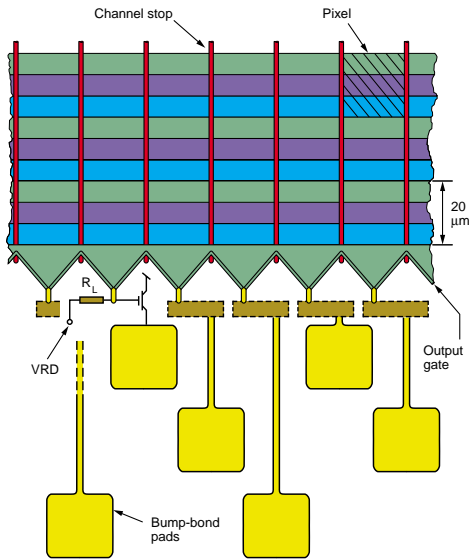
Luminosity and background per bunch are similar.

NLC: CCD readout in 8 ms between bunch trains provides adequate background control

TESLA: **15 times more luminosity per train**, so need to read repeatedly during each train of $950 \mu\text{s}$

→ Concept of **column-parallel readout** in $50 \mu\text{s}$, which is interesting for other CCD application areas.

[An earlier option of fast clear, fast trigger and kicker magnet to kill the bgd was excluded by GMSB and other subtle signatures: the LC DAQ *must* run in an untriggered mode.]

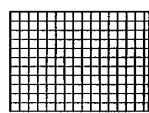


- Maybe no-reset output with resistive load
- Single row of staggered bump bonds follows standard industrial practice
- Goal is 50 MHz parallel clocking with 1-3 V drive voltages
 - what implications for on-CCD buslines, in-detector cooling?
- Signal processing well-matched to 0.25 μm processing. Much can be learned from CMOS active pixel imaging devices

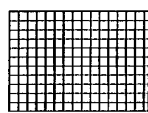


ON-CHIP ADC ARCHITECTURES

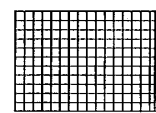
Photobit



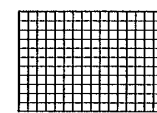
Digitized in pixel



Serial ADC(s) at data rate



Column parallel ADCs Multiplexed output

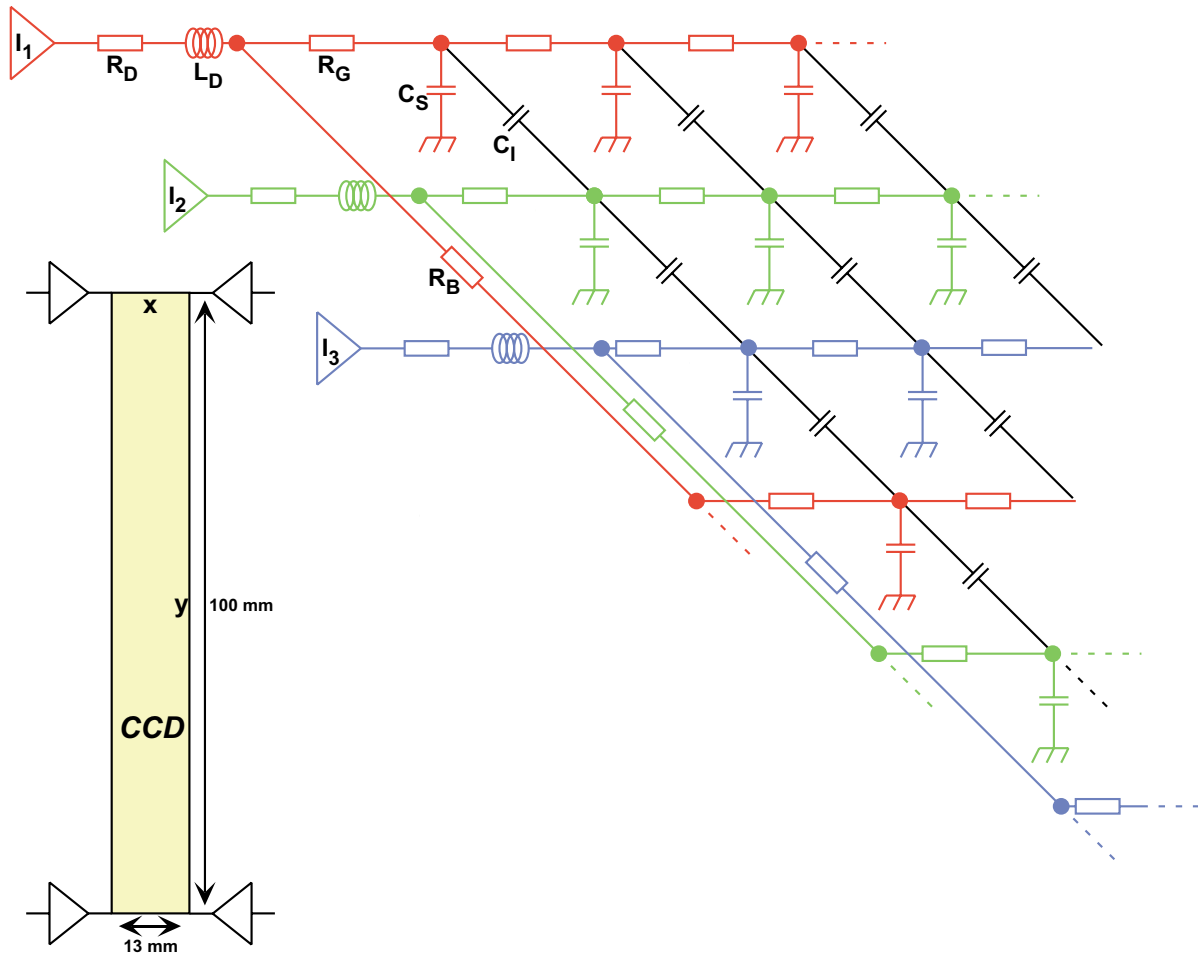


Column parallel ADCs Parallel output ports

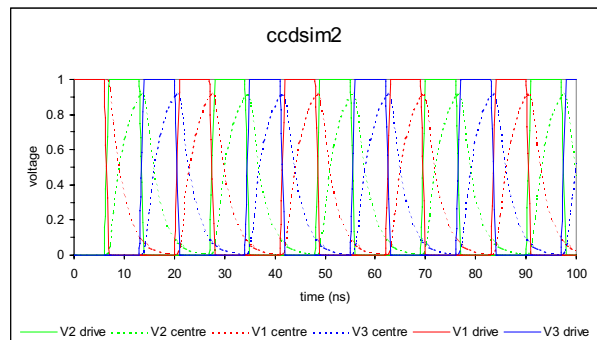
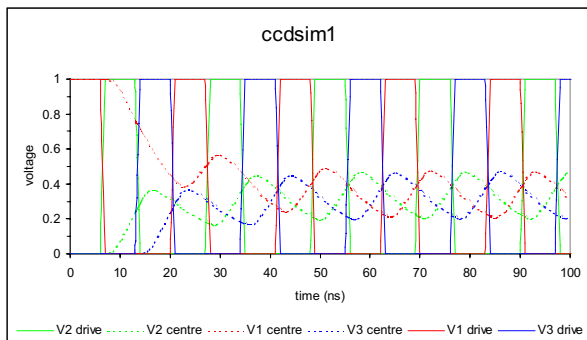


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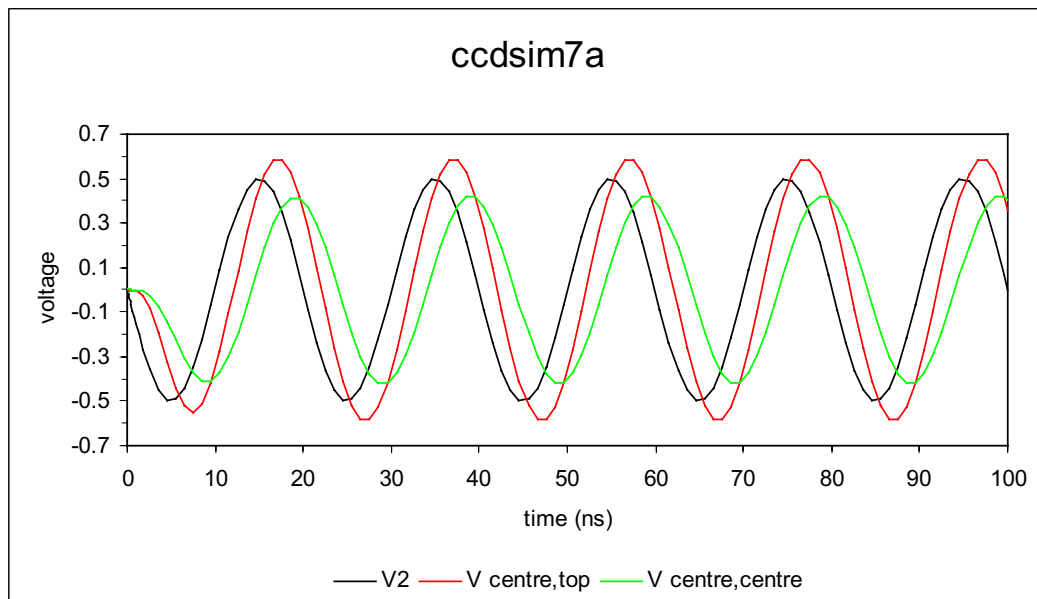
Initial studies based on 3-phase clocking



**SPICE model of column-parallel CCD gate structure
(VXD layer 1 dimensions)**



However, the LC lends itself to 2-phase sinusoidal operation, starting slightly before the bunch train



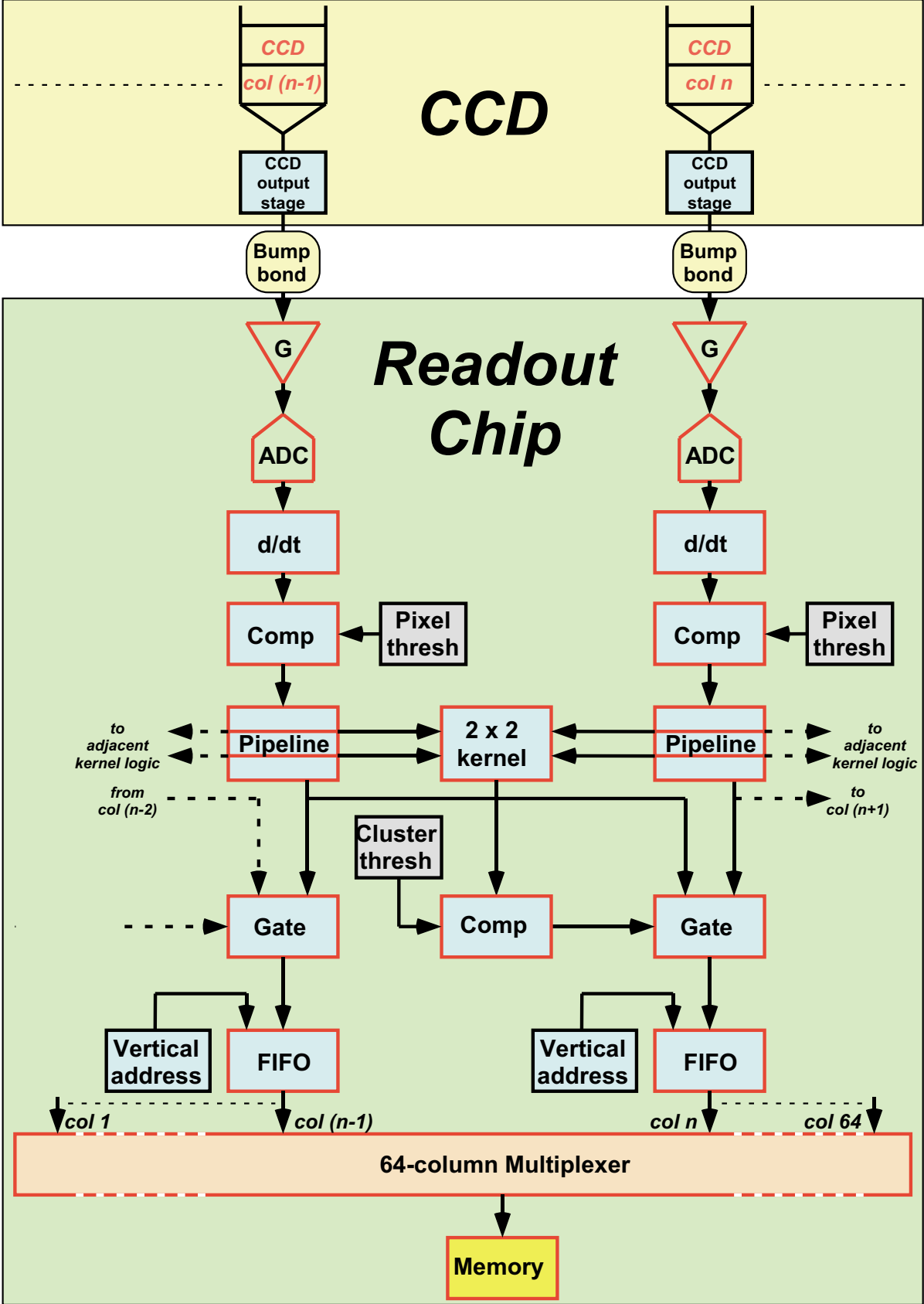
Latest estimates:

In detector power dissipation \approx 9 Watts!

→ a very gentle flow of cooling gas

[Ladder ends will need more aggressive cooling: 'no problem'.]

Readout IC



- Background occupancy 5.9 hits/mm² (layer 1) to 0.6 hits/mm² (layer 5)
 - $\sim 2.6 \times 10^6$ hits/train
 - 15 MB stored on detector during train and read out to a selected available processor between trains
 - a few optical fibres each end

Conclusions

- We have about 5 years of R&D before technology choices need to be made
- CCDs, while promising, could run up against show stoppers such as:
 - present goals achieved too late or not at all
 - manufacturers losing interest
 - radiation environment (specially neutrons)
- For *all* options, CCDs, hybrid pixels and CMOS pixels, important to push hard. Much scope for development; physics prizes could be immense
- All these technologies are in demand for many applications. Developments are likely to make brisk progress into the distant future, independent of HEP community
- The preferred technology may well change during the life of the collider
- Therefore vital to ensure **convenient access** to the inner detector, in order to permit instrumentation upgrades (vertex detector, beamsize monitor, beam position monitors) every few years.