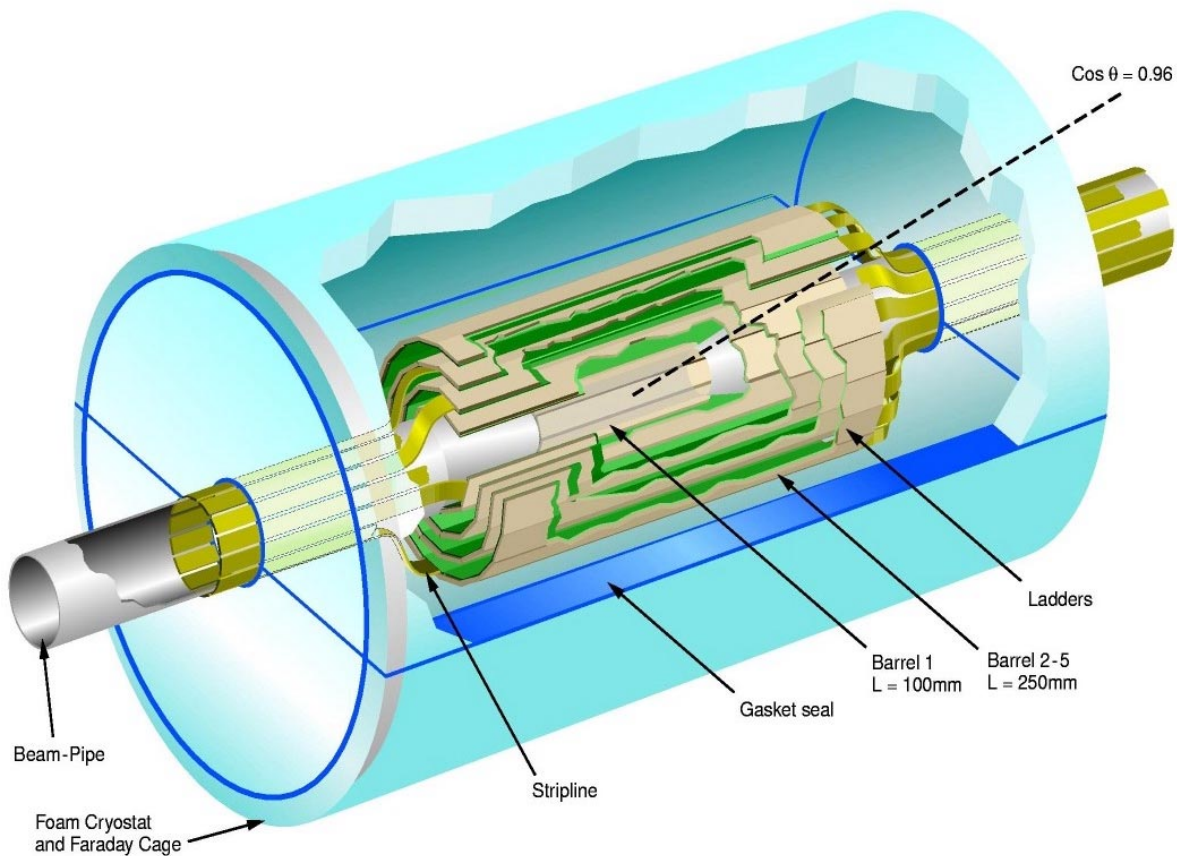


# LCFI Research & Development Programme, Results and Plans

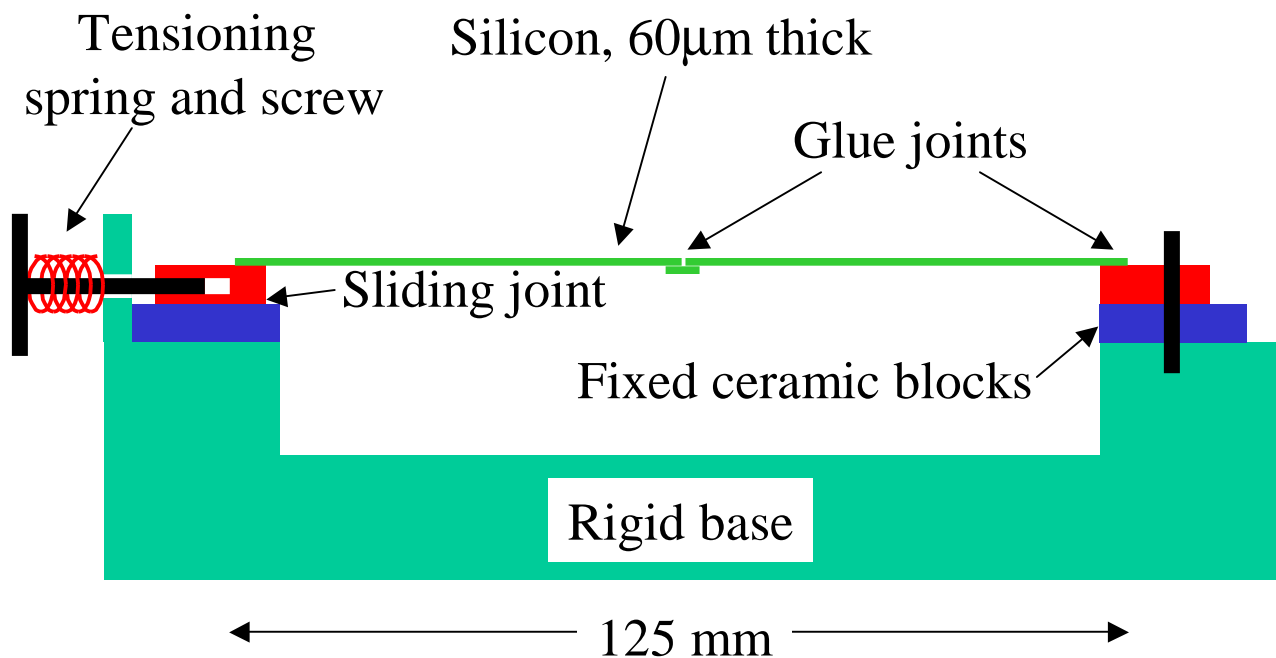
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- Minimising the material budget.
- Operating CCDs at the LC.
  - Radiation damage.
  - Readout speed.
- Future R&D programme.
- Summary and request to PPESP.

# Unsupported CCDs

- Hold CCDs at ends, under tension.
- Particles see  $60\ \mu\text{m}$  of Si ( $0.06\% X_0$ ).
- C.f. world record of  $0.4\% X_0$  to date (SLD vertex detector).
- Stability under temperature cycling?
- Schematic diagram of test rig:



- For various tensions, repeatedly disturb, measure sagitta using ATLAS SmartScope.

# Unsupported CCDs

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- Unsupported Si test rig.

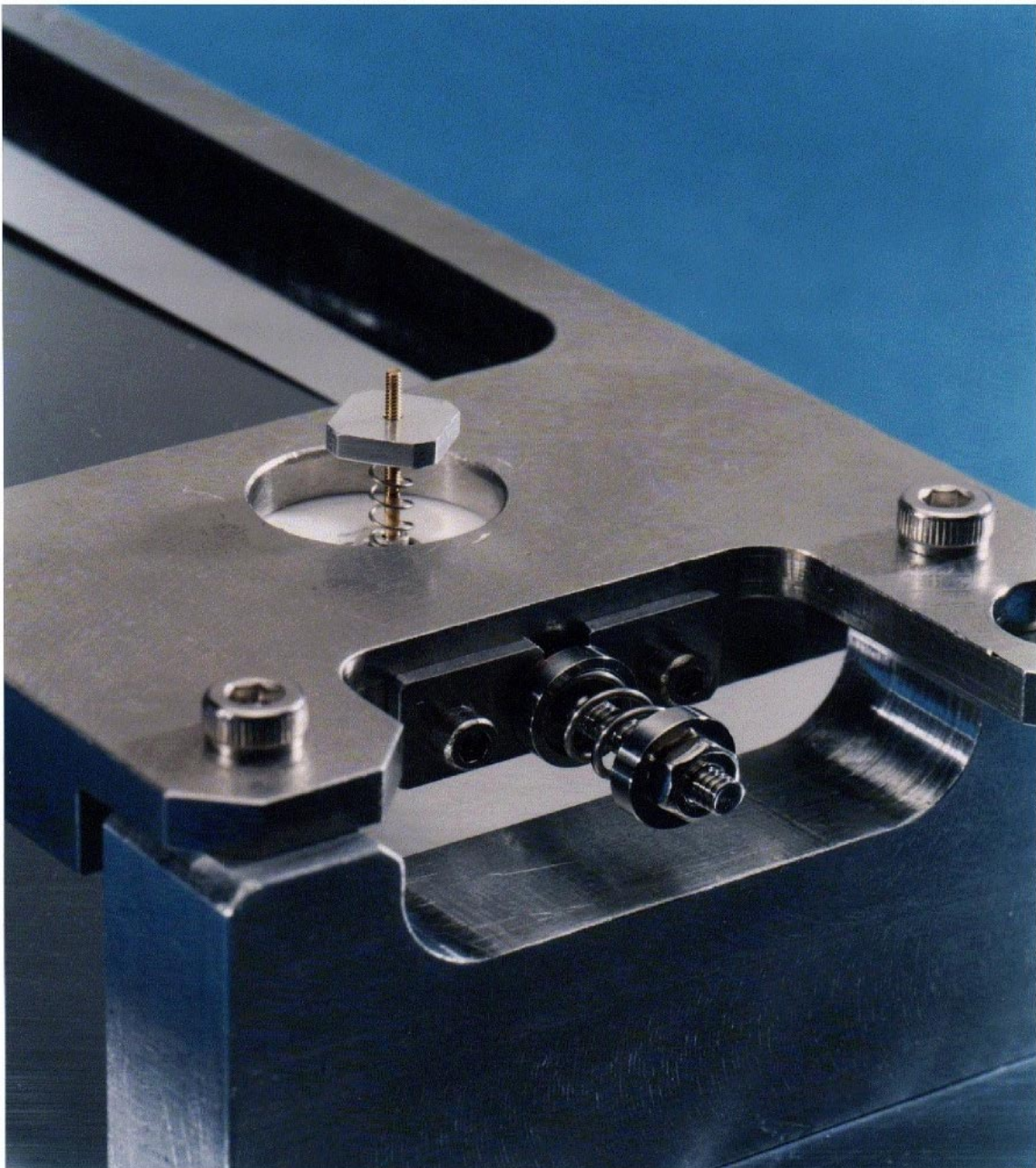




# Unsupported CCDs

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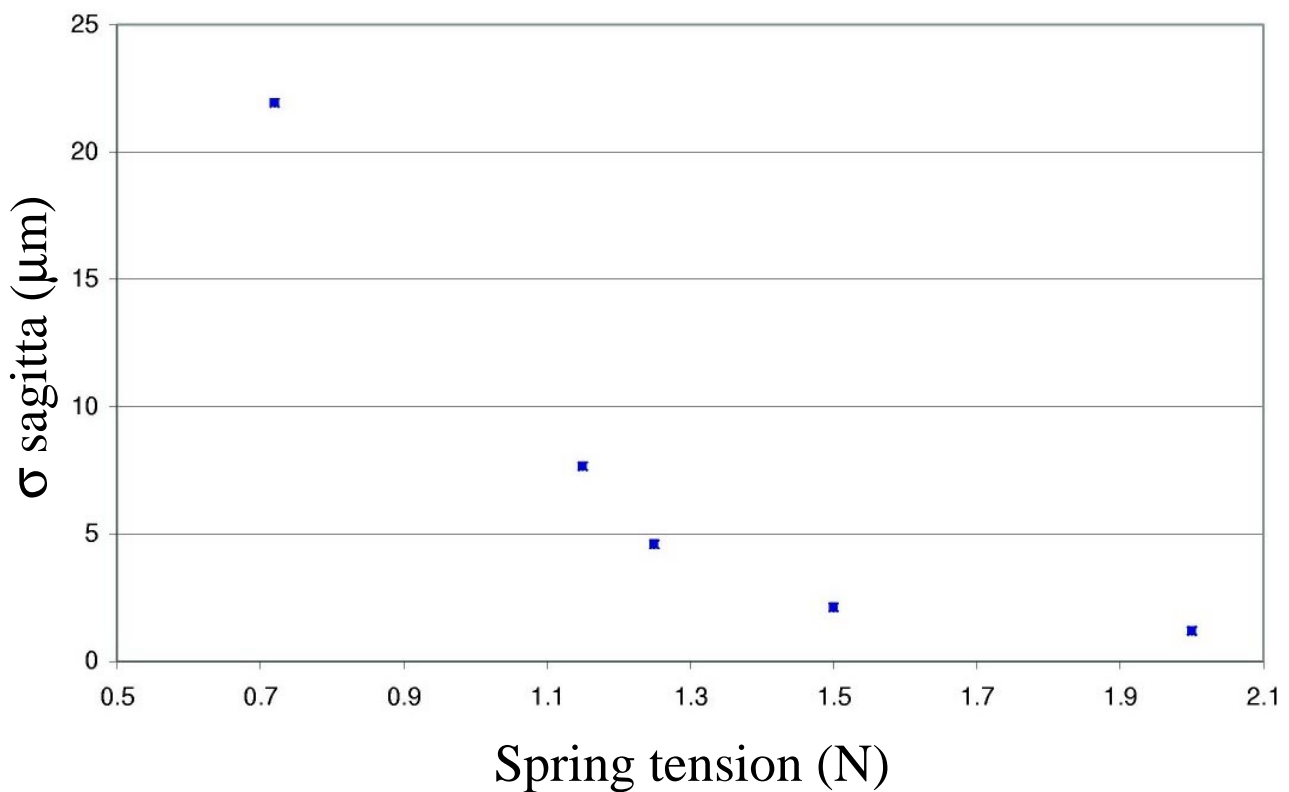
- Detail of Si tensioning mechanism.



# Unsupported CCDs

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- Results:

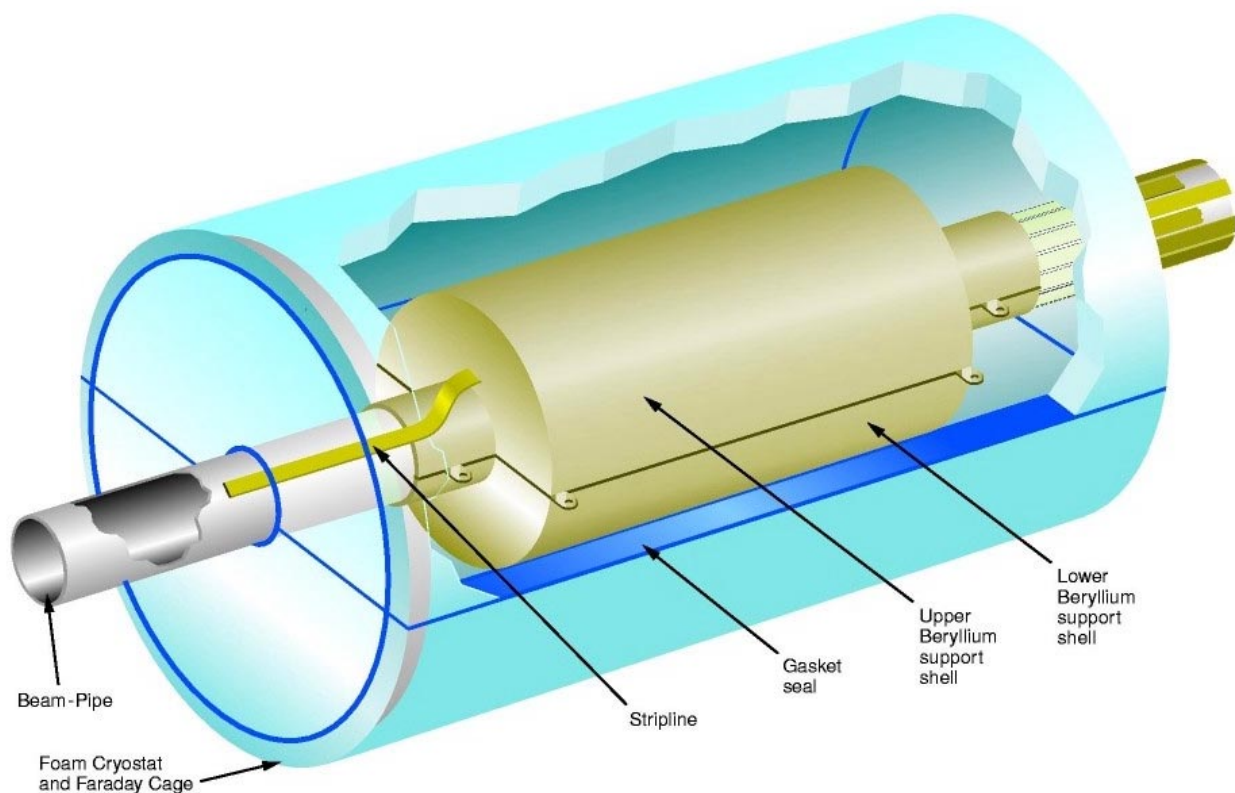


- First studies show  $\sigma \sim 3 \mu\text{m}$  for tension  $> 1.5 \text{ N}$ .

# Unsupported CCDs, VXD design

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- Maintain gains achieved by very thin CCD layers.

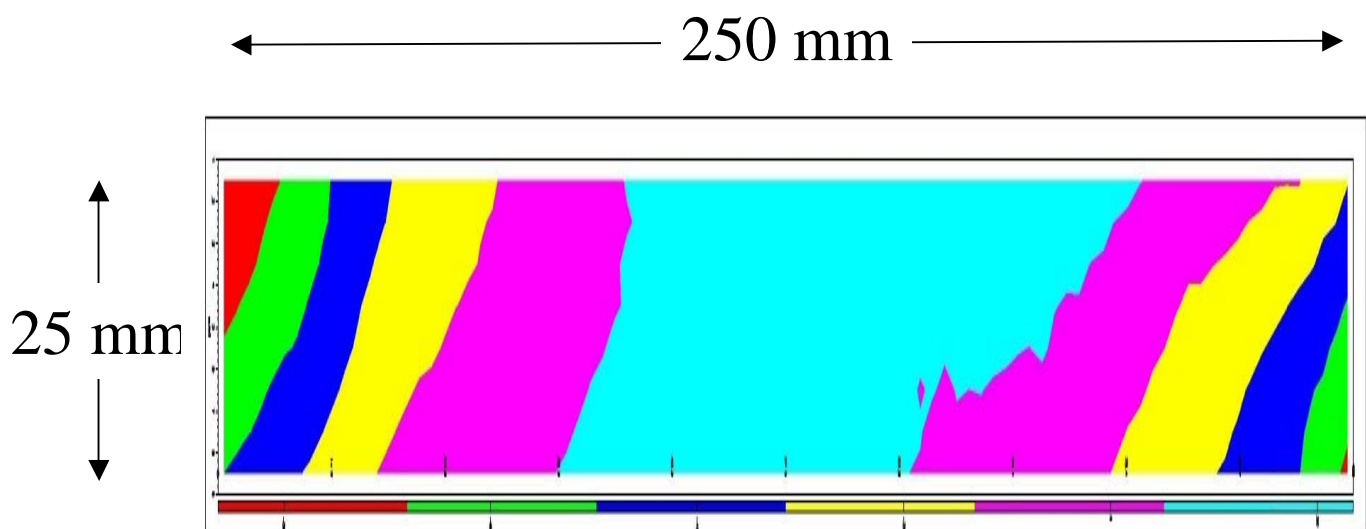


- Be shell outside inner tracking volume, thickness 1...2 mm.
- Beampipe thickness  $\sim 0.25$  mm Be (0.07%  $X_0$ ).

# Surveying CCD ladders

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- Two metrology systems:
  - Upgraded Oxford ATLAS WhIPM system.
  - RAL ATLAS Smartscope.
- Portable LN<sub>2</sub> cryostat for use on either system, study thermal distortions.
- WHiPM profile of dummy ladder (contours at 20 μm intervals, resolution better than 5 μm):





# Surveying CCD ladders

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- Cryostat with cooling system on SmartScope at RAL.

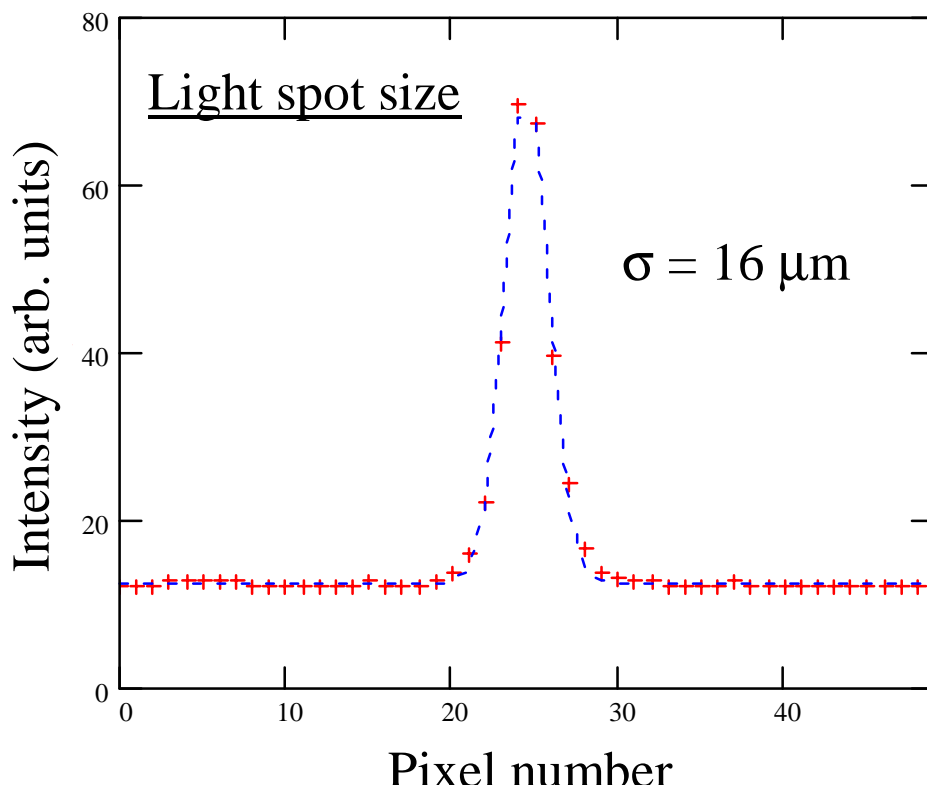




# Operating CCDs at the LC: radiation damage

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- Neutron dose at LC  $\sim 4 \times 10^8$  1 MeV equivalent n/cm<sup>2</sup> and year.
- Conventional CCDs can tolerate  $8 \dots 1500 \times 10^9$  1 MeV n/cm<sup>2</sup> before CTI drops to  $5 \times 10^{-5}$ .
- Column parallel CCDs less sensitive.
- Liquid He/N<sub>2</sub> cryostat constructed at Liverpool with optical charge injection.



# Operating CCDs at the LC: readout speed

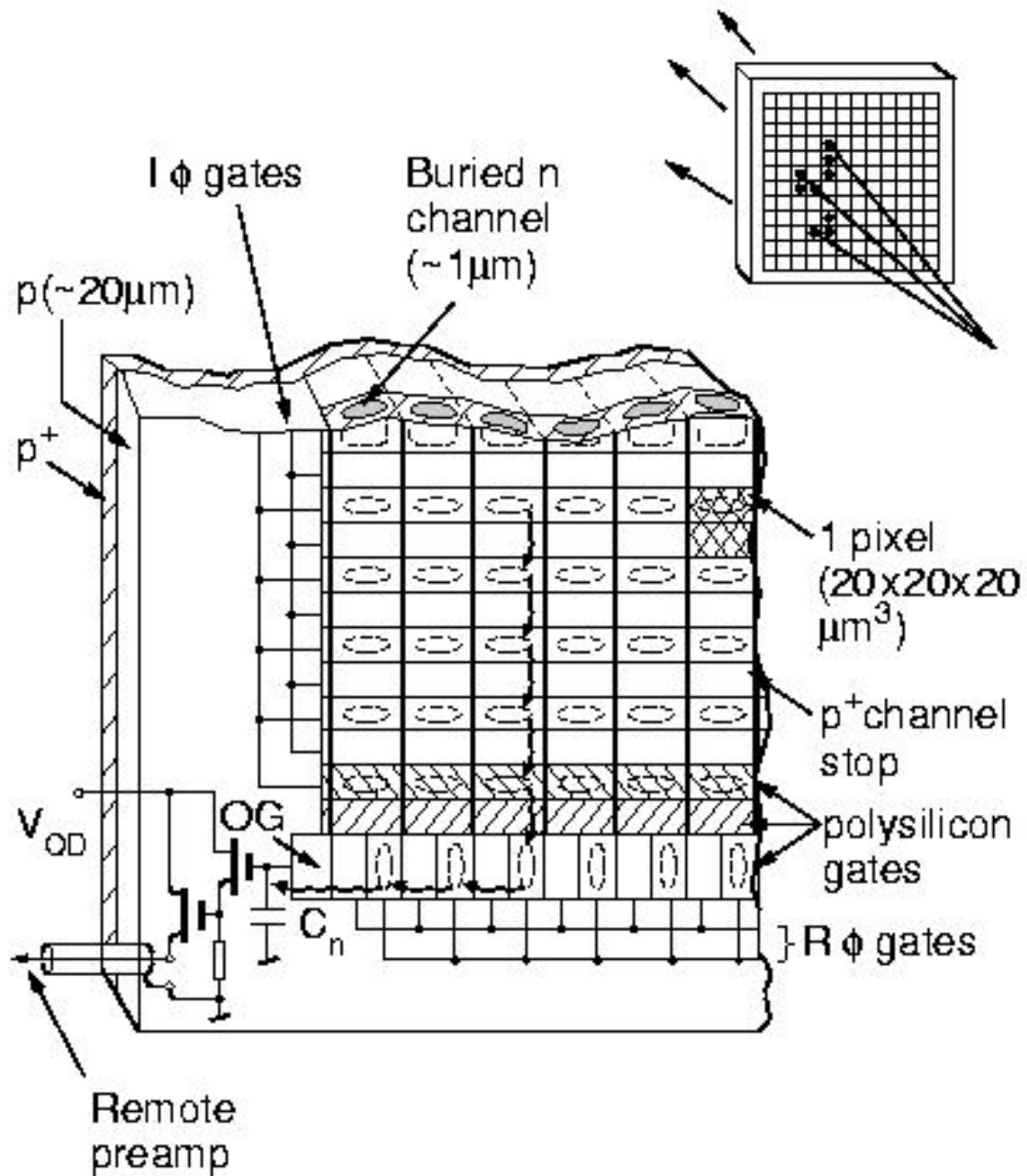
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- Major concern here  $e^+e^-$  pair production.

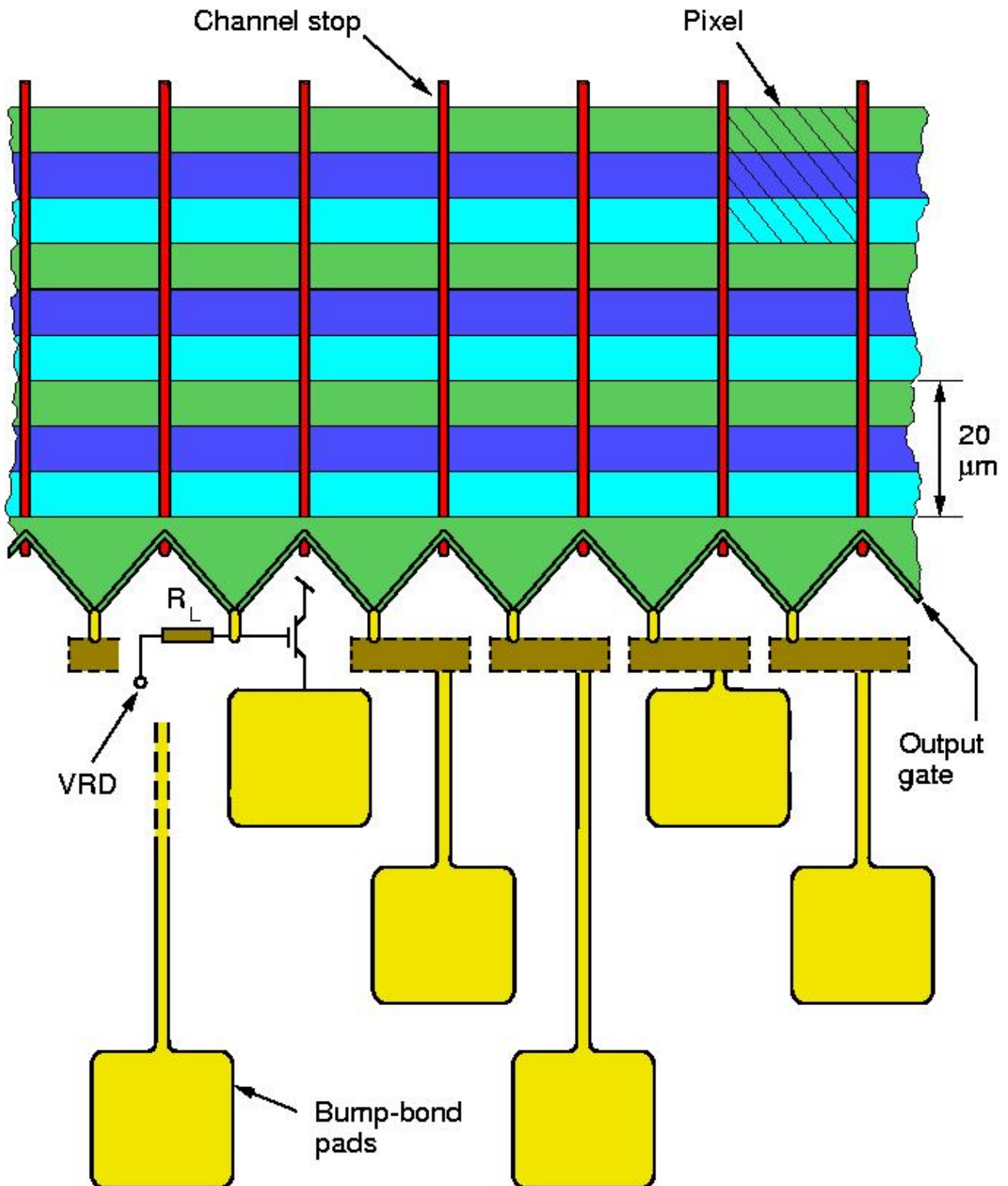
	NLC	TESLA
$\sqrt{s}$ (TeV)	0.3...1.0	0.09...0.8
$\mathcal{L}$ ( $\times 10^{34}$ cm $^{-2}$ s $^{-1}$ )	0.5...3.4	3.4...5.0
Rep. Rate (Hz)	120	5...3
Bunches/pulse	95...190	2820...4500
Bunch sep. (ns)	2.8...1.4	337...189
Radius (cm)	1.2	1.5
Hits (mm $^{-2}$ BC $^{-1}$ )	0.03	0.03
Hits (mm $^{-2}$ BT $^{-1}$ )	4	80

- Must readout TESLA CCDs 10 times per BT to keep occupancy at  $\sim 4$  hits mm $^{-2}$ .
- Need column parallel readout at 50 MHz.

# Conventional CCD



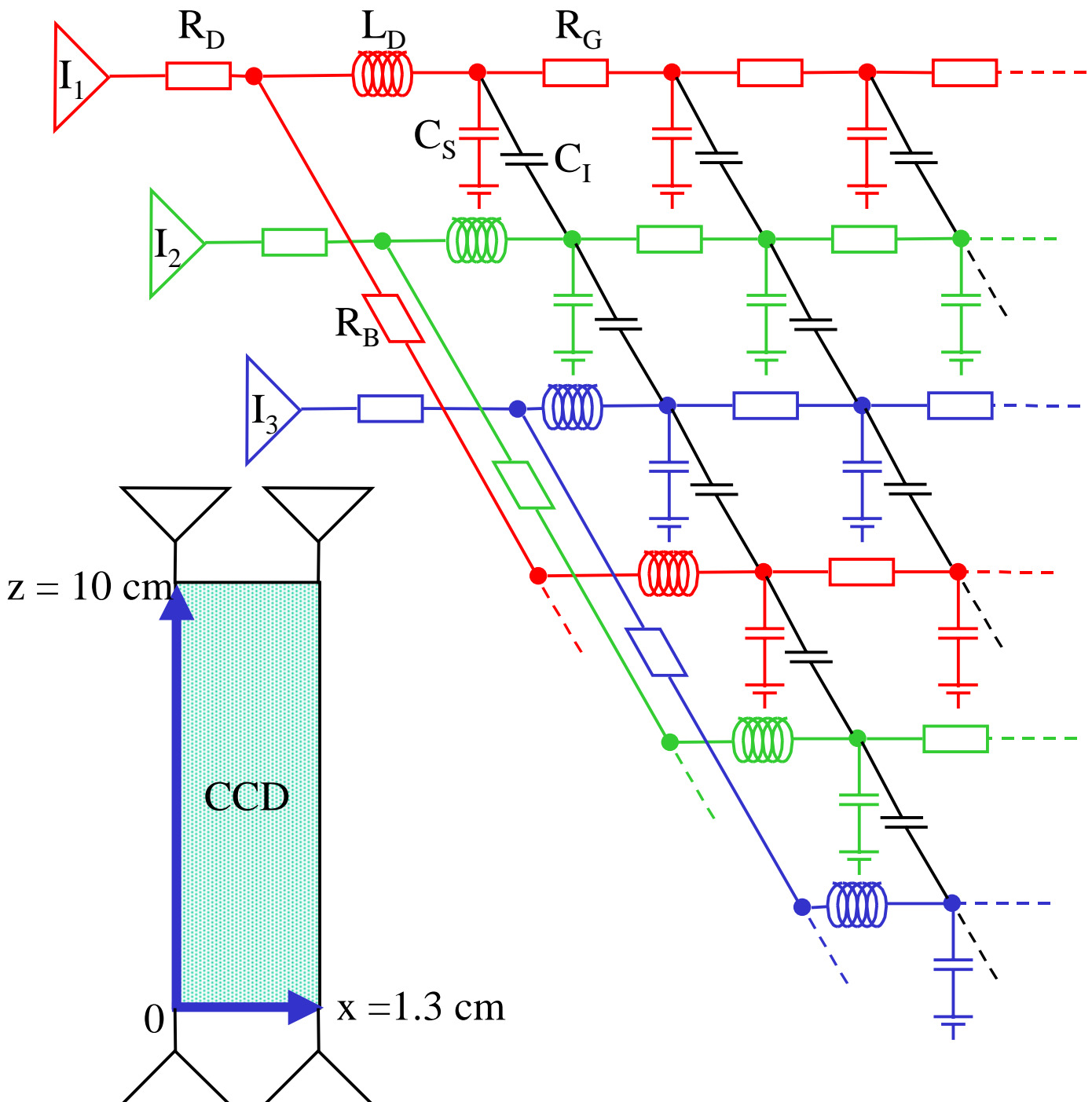
# Column parallel CCD





# SPICE model, inner barrel CCD

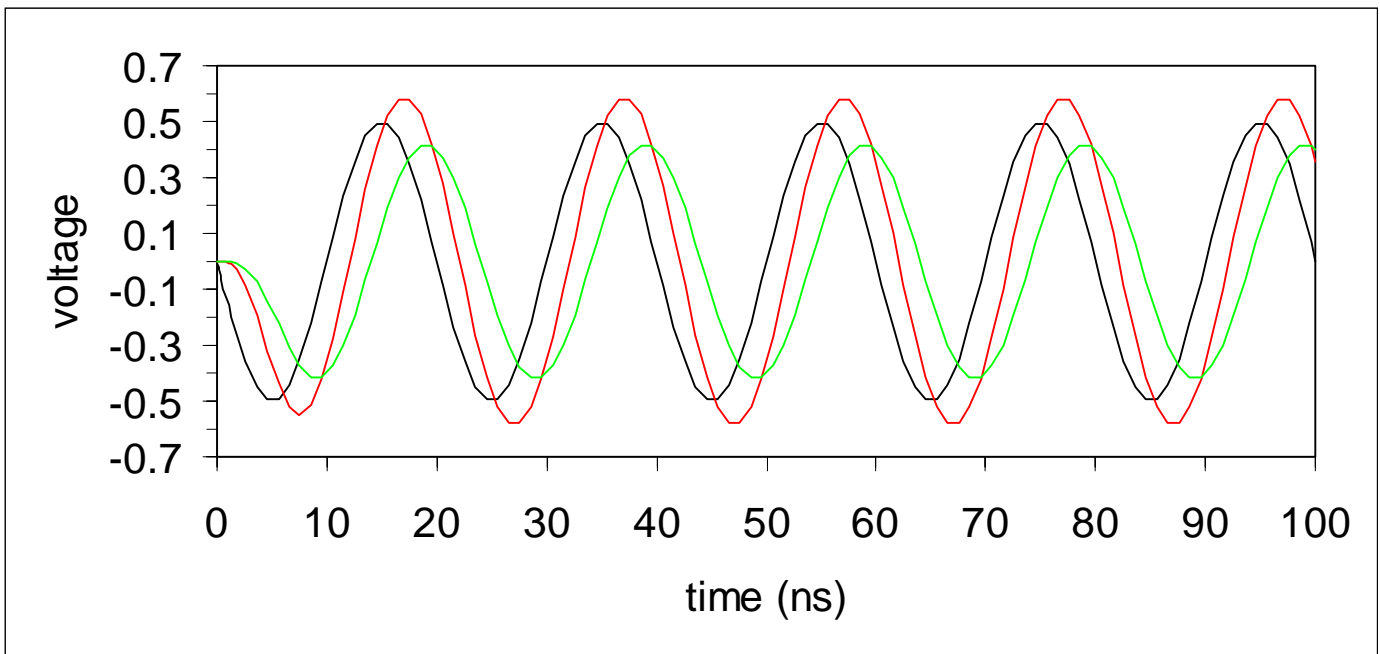
- Can the I gates be clocked at 50MHz?



# SPICE simulation results

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- Reduce gate resistance by addition of 1  $\mu\text{m}$  thick 3  $\mu\text{m}$  wide Al strips.
- Reduce bus line resistance by increasing thickness of Al.
- Try 2-phase sinusoidal drive pulses.



V2 drive                    —————                    V2 centre, centre —————  
V2 centre, top —————

# SPICE simulation results

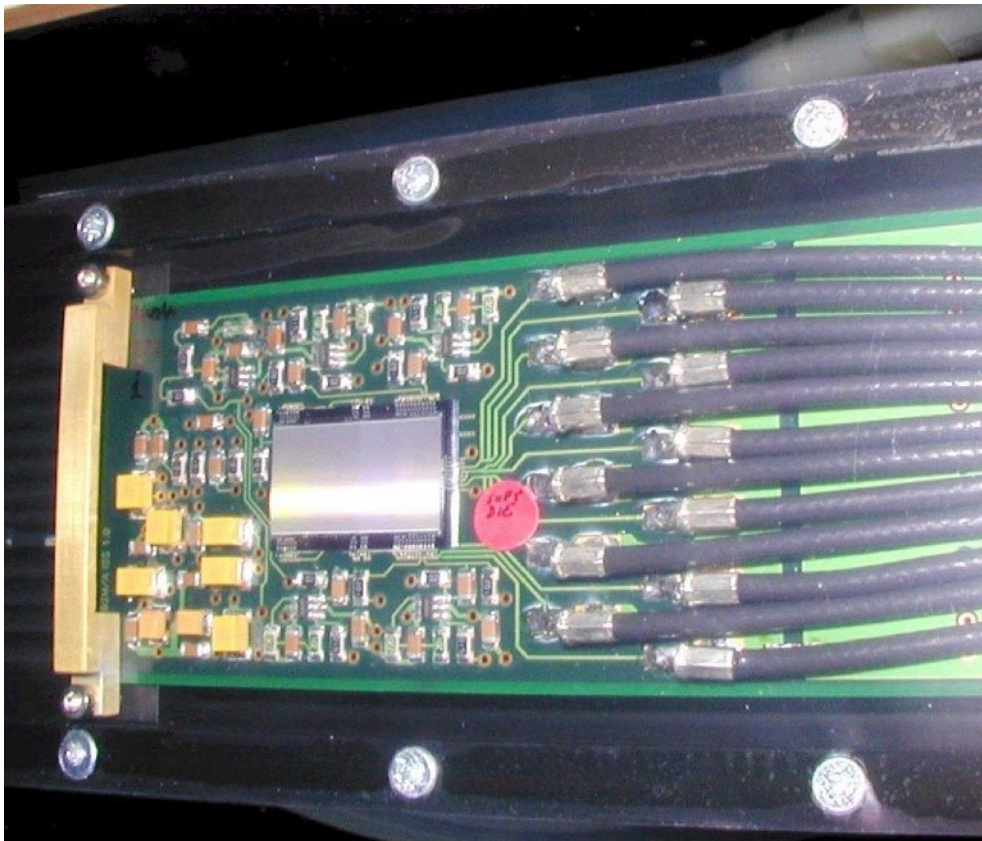
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- Waveforms in centre of CCD adequate for efficient operation.
- Total power dissipation/CCD (continuous operation)  $\sim 4$  W.
- TESLA duty cycle  $\sim 1/200$  and outer CCDs can be clocked at lower frequency.
- Total VXD power consumption is few watts.
- Cooling can be achieved with gentle gas flow.

# Experimental studies of readout

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- VME based 50 MHz drive and readout electronics designed and under construction.
- CCD58 on motherboard delivered by Marconi.



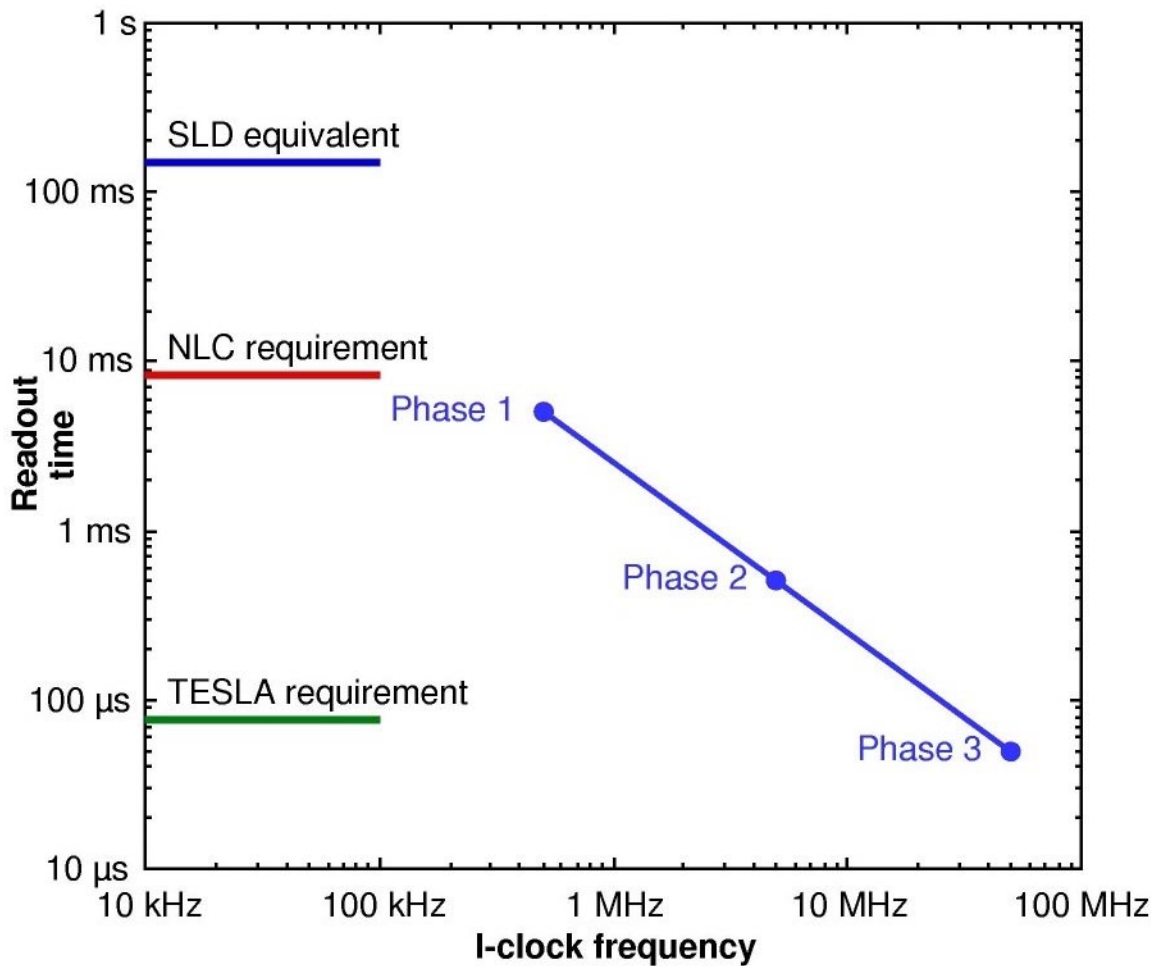
- First tests imminent.



# Future R&D

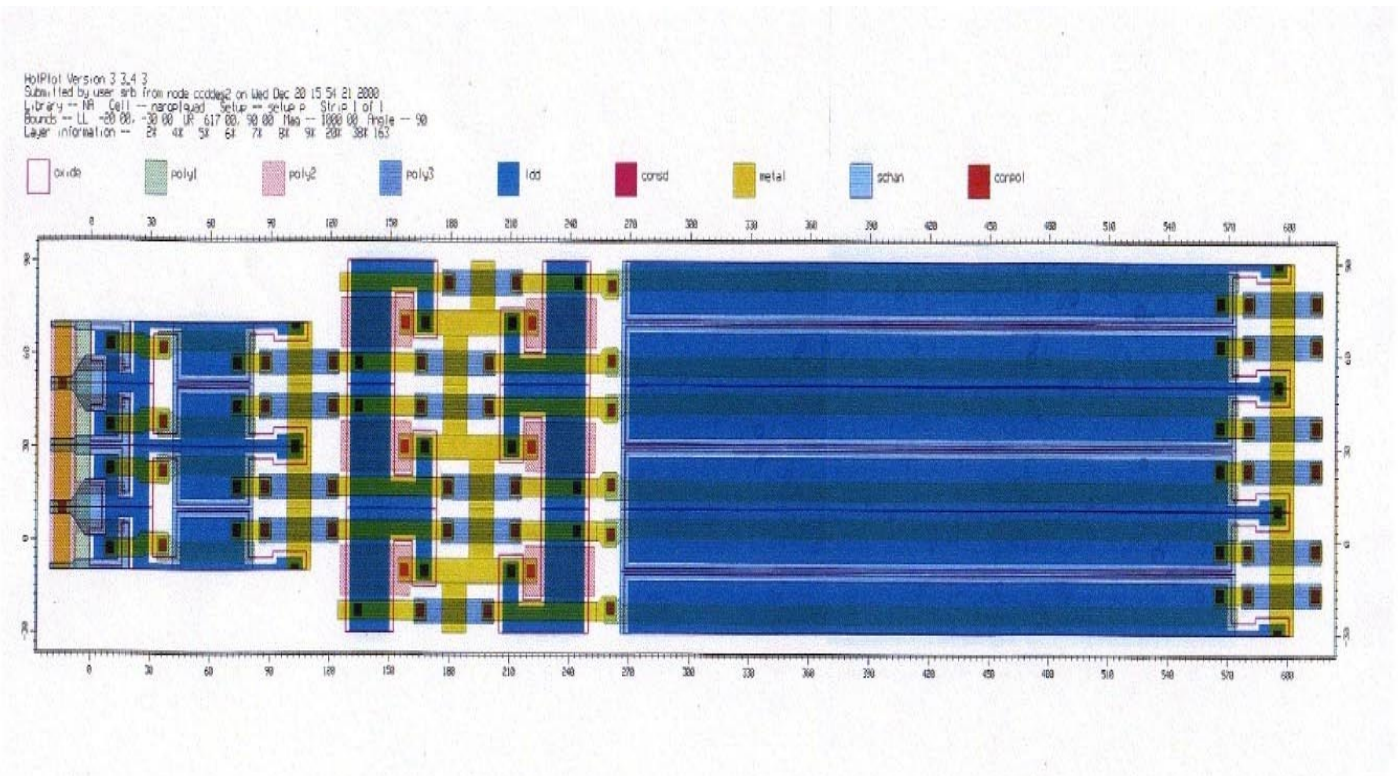
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- Three phase programme proposed:

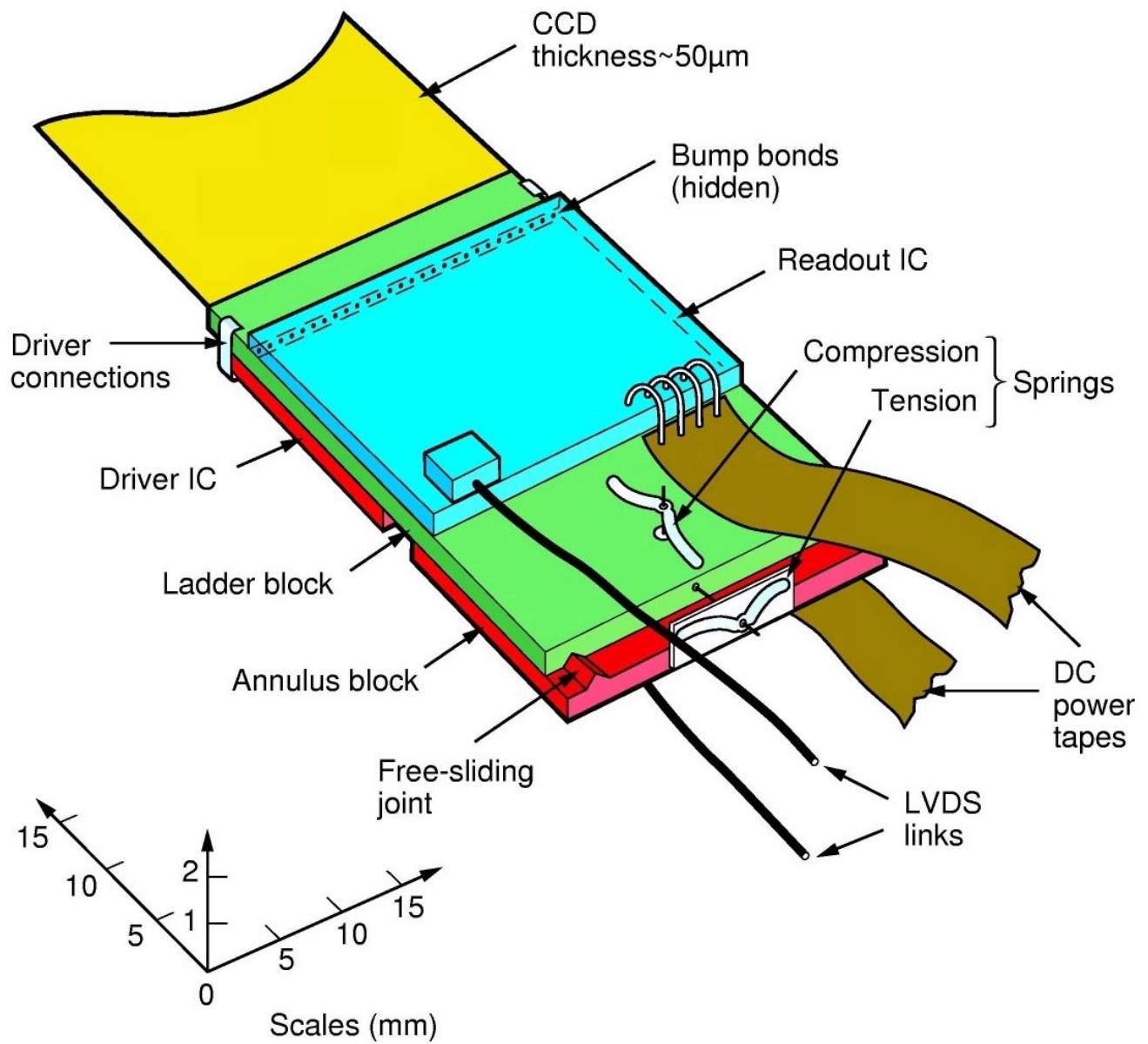


# Future R&D, phase 1

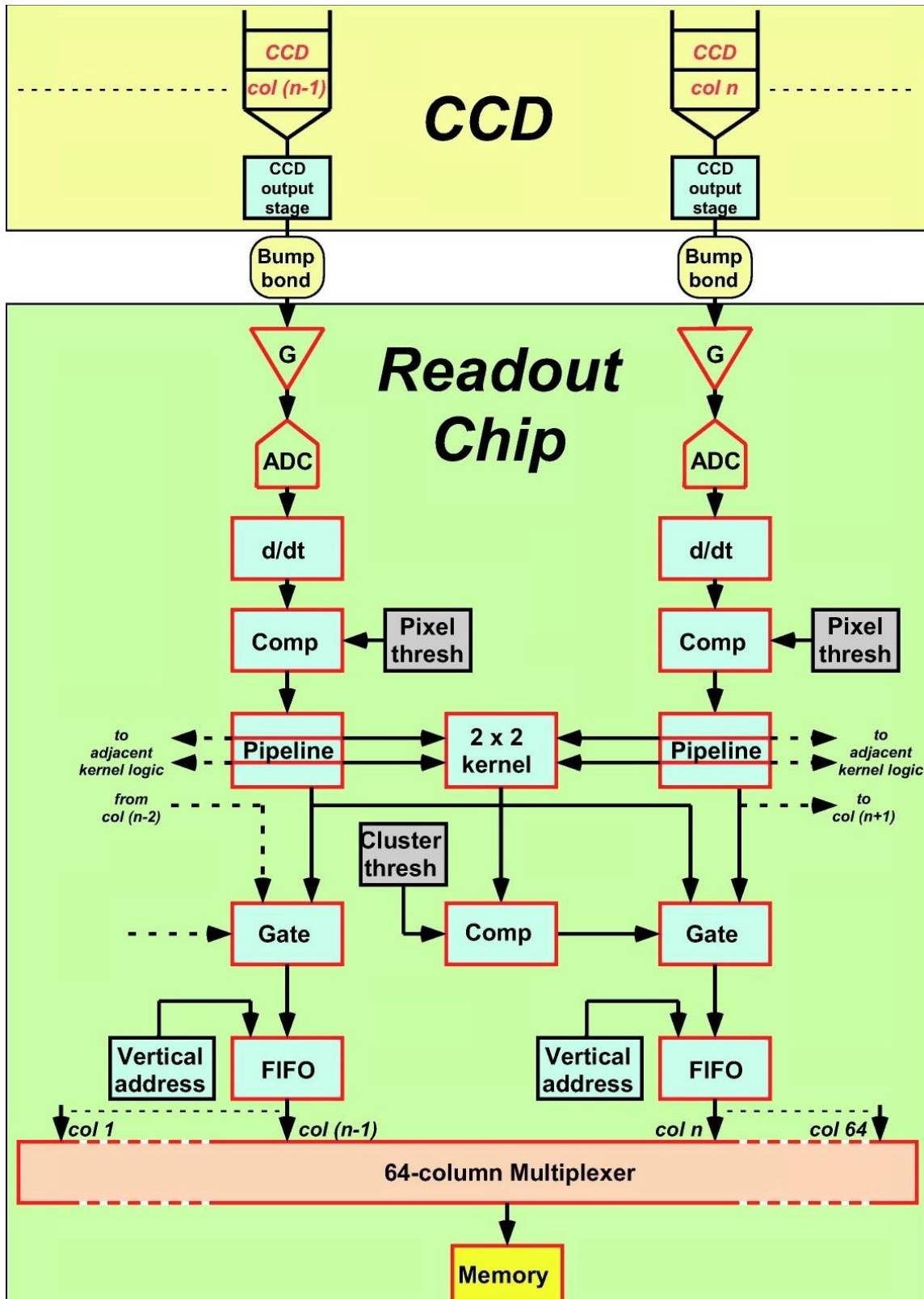
- Move to column parallel readout, but with standard clock frequencies and voltages.
- Main challenge is production of output circuits on pitch of  $20\ \mu\text{m}$ .
- Marconi designed possible output circuit following discussions with LCFI.



# Detail of ladder end



# Readout logic





# Future R&D, phases 2 and 3

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- Increase readout speed by factor 100 in two steps.
- These steps will depend on results obtained in phase one, but 50 MHz operation requires:
  - Metal buttressing.
  - Reduced clock voltages.
- Marconi have proposals for achieving above.
- Guide developments and experimental studies using simulations.
  - Semiconductor devices modelling group at RAL.
  - ISE TCAD at Liverpool.

# CCD modelling

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- First task:
  - Must understand CCD L, C and R for 50 MHz operation.
  - C and R known.
  - Simulation of CCD needed to find L.
  - Develop test structures to measure L.
- Later:
  - Produce full 3D simulation of minimum ionising particle charge collection and transfer in 4 T magnetic field.

# Summary of progress to date

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- The LCFI collaboration has made significant progress in the last two years:
  - The VXD design goals are now clear.
  - Test rigs are now available.
  - 50 MHz capable drive and readout electronics are available, with final systems expected within months.
  - First CCDs obtained from Marconi.
  - Simulation studies advancing.
  - Unsupported silicon tests successful.

# Future plans

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- A three phase and four year programme has been developed which will provide:
  - Studies of LC physics involving flavour identification.
  - Column parallel CCDs meeting the specifications necessary for the NLC and TESLA.
  - Thin unsupported CCD ladder structures.
  - High speed readout and driver chips.
- These developments will be useful for SR imaging, space-based applications and time resolved spectroscopy in addition to HEP.