Linear Collider Flavour ID (LCFI) Collaboration

P306 – Current status and funding request
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1 Current status

(a) Thin ladder development

- *Test system*. Fully operational facility for precise measurement of ladder profiles as function of temperature, on recovery from mechanical disturbances, etc.

- *Simulations.* Full FEA system used to guide the experimental programme, cutting down the number of engineering models needing to be assembled and tested.

- *Unsupported (stretched) silicon.* Tests with 60 micron thick unprocessed silicon have reached a high performance level. However, due to differential contraction on the processed surface of a real CCD, simulations suggest that curvature across ladder width may be excessive. Experiments with CCD-processed silicon are beginning.

- *Partly supported silicon*. 20 micron silicon on 250 micron beryllium (stretched) looks promising in simulation. Would be a very acceptable fallback for physics. Experiments beginning.

(b) Fast CCD readout

- *Test system*. Fully operational facility for CCD testing in Lab 9 at RAL.

- 15 MHz pixel clocking rate achieved with CCD58 (conventional architecture). May reach tens of MHz when high speed drivers are installed next month. Valuable learning curve for column parallel CCD.

(c) Column Parallel CCD (CPCCD) project

- *CCDs.* Preliminary design is expected to be completed on schedule, 3rd December. Moving to detailed design and production. Thanks to many new ideas, these first devices will be used to explore a variety of design options, as well as several processing options, enabling the project to cover critical aspects of all the Phases 1-3 of the PPESP proposal of 19th March 2001.

- *Readout IC.* Exploring novel ideas for interface between CCD and readout chip. Conceptual design of readout IC is complete. Detailed design proceeding quickly.

- *Bump bonding.* A clear plan has emerged in close consultation with VTT in Finland. This essential part of the project will establish whether the column parallel concept is valid. Critical issues such as noise performance, high speed operation and CCD drive clock feedthrough to the hundreds of analogue outputs are layout-sensitive, and cannot be resolved in wire bonded assemblies.

- *Driver electronics.* Study under way, including simulation of all inductances on and off the CCD. A major goal is to achieve extremely low power operation.

(d) Physics studies

- Code developed within the LCFI collaboration is now being supplied to the entire TESLA community, as it is the highest performance flavour ID package available.

- Next step will be the international version, following a recent successful meeting in CERN on global standardisation of LC simulation and reconstruction tools.

- Physics studies are closely coupled to the detector design; will be helpful in deciding between different pixel detector options in 4 or 5 years time. Currently, all of CCDs, monolithic APS and DEPFET pixels are serious candidates for LC vertex detectors, and are the subject of vigorous R&D programmes round the world.

2 Plans through FY 02/03

- Experiments with fast CCDs (conventional architecture) will soon be completed.

- Thin ladder development will continue long term. This part of the R&D programme is important for all pixel-based vertex detector options, and is relatively inexpensive.

- First CPCCD assemblies will be completed mid 2002, initially with wire bonded readout chips then bump bonded.

- Drive pulse propagation over CCD area will be studied with an existing probe station.

- Full device operation will then be studied in the existing CCD test facility at RAL.

- Latter half of FY 02/03 will be devoted to an in-depth evaluation of the various CCD architectures produced by MTech.

- Radiation damage studies of CPCCD will begin at Liverpool U.

3 Funding request

Remainder of FY 01/02

Continuation at modest level (two FTEs) from RAL Instrumentation Dept to complete readout chip design, to participate in driver design, and in thin ladder R&D.

£88K (£75K + VAT) for MTech to complete CPCCD detailed design

FY 02/03

Thin ladder development	£17K
CPCCD manufacture £150K + VAT	£176K
Readout ICs manufacture	£17K
Drivers / mbds and VME readout	£10K
Bump bonding	£32K

Note that this request assumes a funding pause with MTech and RAL Instrumentation Department from October 2002, while the first generation devices are tested. The design of second generation CCDs and readout ICs would thus be deferred till FY 03/04. We think this should be acceptable, unless some unexpected global problem is encountered in the first devices.

Our equipment request for FY 02/03 of £252K has been pared down drastically from the figure of £541K in our proposal of 19th March 2001. This reduction has been achieved by the abovementioned funding pause, and by the development of a more cost-effective strategy for the bump bonding. The modest manpower request from ID reflects the strong role now taken by Oxford University mechanical and electronic engineering in the project.

We believe our request to be the minimum figure needed to keep the project alive, though it is not of course mandatory that the funding should be provided entirely by the PPRP. We hope that the global PPARC budget will prove sufficient to maintain this project at a viable level, particularly since PPARC has placed a high priority on UK participation in the future LC once it coalesces into an international project. In the meantime, we hope they will wish to maintain viability of the UK activities in this area, just as the other countries supporting the future LC are doing. Not to do so would be to pull our collaboration out of the running just before the start of this major new international project.

We should emphasise that the work of FY 01/02 and 02/03 represents the first step in a long term R&D programme. In order to realise the LC vertex detector, we will be dependent on further developments in the technologies of CCDs, scaled CMOS as it evolves for mixed mode devices, and power electronics. As happened with the LHC pixel detectors, convergence of the R&D programme over a five-year timescale is a reasonable goal. For FY 03/04, we would expect a period of say three months for design revisions of CCD, readout IC and driver, followed by a six month production phase. The budget required for FY 03/04 might be 30% higher than for FY 02/03.