Status Report and Proposal for Extended R&D for a Vertex Detector at the Future e^+e^- Linear Collider

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Linear Collider Flavour Identification Collaboration (LCFI Collaboration: http://hep.ph.liv.ac.uk/~green/lcfi/home.html)

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Abstract

The LCFI collaboration started work in October 1998 after PPESP approval for an exploratory R&D programme. After two and a half years, the prospects for physics at the future linear collider have clarified significantly, partly due to the work of this collaboration. It remains apparent that a vertex detector with an extremely high performance specification will be an essential tool for physics at the TeV scale, both for precision measurements and for particle searches in the SUSY and other sectors. Over the past two years, various developments with respect to background studies, DAQ requirements (triggerless operation) and technological progress (paper-thin packages, PTPs) have significantly changed the prospects for an optimised vertex detector design. The LCFI collaboration considers a CCD-based architecture, building on the 307 Mpixel SLD vertex detector, as being the most promising technology option. We therefore propose to extend the R&D programme in order to develop this technology within the next 4 years to meet the physics requirements. Achieving these goals will require an effective readout rate 30-1000 times faster than in SLD, depending on the LC accelerator technology selected. We propose a three-phase R&D programme, each step of which will yield significant spinoff to those other areas of scientific imaging that are limited by the readout speeds available with current CCD technology.

1. Introduction

LEP, SLC and the Tevatron have established the importance of vertex detectors in understanding the physics accessible at high energy colliders. At the future linear collider (LC), both precision measurements and particle searches set stringent requirements on the efficiency and purity of the flavour identification of hadronic jets, since final states including short-lived *b* and *c*-quarks and τ-leptons are expected to be the main signatures. High accuracy in the reconstruction of the charged particle trajectories close to their production point must be provided by the tracking detectors, in particular by the vertex detector (VTX) located closest to the interaction point, in order to perform the reconstruction of the topology of secondary vertices in the decay chain of short-lived heavy flavour particles in a complex environment. High efficiency is essential due to the small event samples in individual processes, and high purity is required because of the generally high backgrounds to many processes of interest.

Experience at LEP and SLD shows the way forward. Jet flavour identification can be based primarily on the topological vertex structure in the jet, since this in principle allows most *B* and *D* decay modes to be detected. By aiming for good sensitivity down to decay times short compared with the mean lifetimes, high efficiencies may be realised. Distinguishing clearly between *b* and *c* jets requires additional information. This comes from the secondary and tertiary vertex topology, the charged decay multiplicity and the vertex mass, after applying corrections for missing neutrals [1].

As well as tagging *b* and *c* jets, the vertex charge (if non-zero) can distinguish *b* from $\overline{b}$, *c* from $\overline{c}$. This requires sufficient precision to distinguish between all the decay tracks and those coming from the primary vertex. Even the case of neutral *B* decays can often be handled by measuring the charge dipole between the secondary and tertiary vertices, as demonstrated in SLD.

Cases where leptons (and hence neutrinos) are absent from jets are particularly valuable for precise jet energy measurement. However,the absence of a single electron in a jet is not so easily established. Due to the prevalence of gamma conversion, it is important to track detected electrons inwards through the thin layers of the vertex detector to establish if they were really produced in semileptonic *B* or *D* decays. As well as providing a clean sample of jets free of missing neutrinos, this procedure in principle allows corrections to be applied to jets with charged leptons (hence also neutrinos). In these cases, the jet energy measurement may be improved substantially by extending the procedure used for the p_T-corrected mass, allowing a correction for the transverse momentum of the missing neutrino.

The overall conclusion from extensive studies of the machine-detector interface is that by careful control of backgrounds, the LC interaction region can be made particularly favourable for the operation of a vertex detector of unprecedented performance, well-matched to the physics goals of the TeV regime.

Since the formation of the LCFI collaboration in October 1998 after PPESP approval for an exploratory R&D programme, we have played an active part in the ongoing international physics and detector studies related to flavour identification and vertex detectors. Of the 5 detector options currently being studied (all of them pixel-based) it is our opinion that a CCD-based design, building on the 307 Mpixel SLD vertex detector, is the most promising. We therefore propose to extend the R&D programme to develop this technology within the next four years to meet the requirements for physics.

In Section 2, the present CCD-based conceptual design is discussed. This has been significantly influenced by developments in the international studies over the past two years. In Section 3, we describe progress made in the LCFI R&D programme since PPESP approval, and in Section 4 we discuss the proposed future programme. This will be divided into three phases. Phase 1 is aimed at achieving performance matched to the NLC detector option, with column-parallel operation at 0.5 MHz. In phase 2, the readout rate will be increased by a factor 10, widening the scope for CCD applications in a number of

scientific fields. Phase 3, aiming for 50 MHz operation, will require the development of reduced clock voltages, reduced gate resistances, and full understanding and control of parasitic inductances. Success with this goal will yield a technology matched to the TESLA requirements.

The LCFI web page provides access to all collaboration publications and talks which are listed in the appendices. The full list of participants and their time devoted to this project, and the request for support for the next 4 years (budget and manpower) are also included as appendices.

2 Vertex detector conceptual design and performance

2.1 Machine-related issues

The most important machine-related parameter which directly impacts on the flavour-ID potential of the detector system is the beam-pipe radius. This was already much better at SLC than at LEP (24 mm as opposed to 50 mm. The lessons learned at SLC have since led to much more advanced beam delivery and final focus system designs, with the result that both NLC and TESLA will permit beam-pipe radii below 15 mm with negligible background related to synchrotron radiation. What can of course not be avoided is the e^+e^- pair background from the beam-beam interaction, but the effects of this background can be limited by the use of a high field solenoid. For TESLA, an inner-layer vertex detector at a radius of 15 mm can have an active length of $\pm$ 5 cm, giving excellent polar angle coverage to $|\cos\theta| = 0.96$ as shown in Figure 1. The average background hit density per bunch cross (BX) is 0.03 hits/ mm^2.BX. Results are similar for NLC.

At the time of the original LCFI proposal, it was planned to provide the LC detector systems with a fast (level 1) trigger, which would have permitted control of these backgrounds in the vertex detector by a combination of fast clearing and a kicker magnet to kill the background during readout, as used in the NA32 experiment [2]. However, it became apparent by the end of

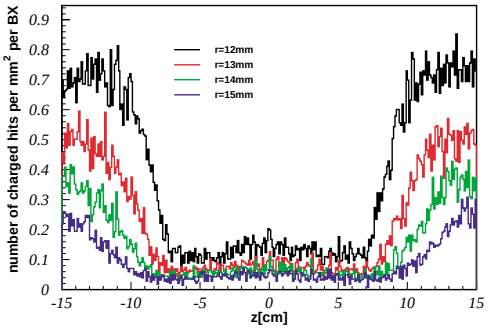


Figure 1: Pair background at the TESLA IR as function of Z position for various detector radii and a solenoid field of 4 T.

1998 that this was not a good idea. Subtle event signatures due to possible new physics (for example, a non-pointing gamma from the decay of a long-lived particle such as could be found within the theoretical framework of gauge-mediated supersymmetry) would need the full event reconstruction to be seen. For this reason, the detector systems will have to absorb the full background. In the case of NLC, the integrated background during the fast train of 190 bunches at 1.4 ns interval is modest, and it is sufficient to read the data out in the 8.3 ms between bunch trains. For TESLA, the long train of 2820/4500 bunches at 500/800 GeV would produce excessive background in a static detector, so multiple readout during the 950 μs bunch train is required. The proposed solution gives a readout time of 50 μs, which is sufficient to limit the pair background on layer 1 to the comfortable level of 4 hits/ mm^2.

Apart from the question of hit density due to the background particle flux, one has also to consider the question of radiation damage. The dominant background (pair-produced electrons which penetrate the VTX inner layer) imposes a requirement on radiation hardness of about 100 krad for a 5 year life, which is easily achieved with modern CCD technology. Potentially more serious is the neutron background. This is currently estimated to be of the order of 10^9 1 MeV-equivalent neutrons/ cm^2. year, which is acceptable with current CCD designs, and there is scope for major performance improvements in these designs, which could produce a large safety factor in radiation tolerance. Such studies

form an important part of the LCFI future R&D programme discussed in Section 4.

2.2 Detector conceptual design

While the background levels require a reasonably find-grained pixel detector at small radii, the hit densities within the core of high energy jets provide an even stronger constraint. With a 10-15 mm inner layer radius, it has been demonstrated [3] that pixels of size well below $50\times50\ \mu\text{m}^2$ are required to avoid serious cluster merging within the cores of jets. The suggested CCD detector design, based on $20\times20\ \mu\text{m}^2$ pixels, is sketched in Figures 2 and 3. The inner 3 layers extend to $|\cos\theta|$ = 0.96, with 5-layer coverage to $|\cos\theta|$ = 0.9. The outer 4 layers are used for stand-alone track reconstruction. The advantages of stand-alone reconstruction in tracking sub-detectors are well-established; they include internal alignment optimisation, efficiency monitoring of the outer tracking systems and vice versa, optimal identification of γ conversions within the vertex detector and optimal rejection of 'bad' hits due for example to cluster merging between signal and background hits.

Having found the tracks in layers 2-5 (and rejected a low level of fake tracks by linking to the outer tracking detectors) the layer 1 hits are used solely to refine the track extrapolation to the IP, which is particularly important for low momentum particles.

Figures 2 and 3 show the detector inside its low-mass foam cryostat, used to permit an operating temperature of around 180 K. Figure 4 shows the high precision mechanical support structure (a closed pair of beryllium half-cylinders) which is mounted off the beam-pipe inside the cryostat. Being outside the volume used for the precision measurements and extrapolation to the IP, this cylinder can be relatively robust (1-2 mm wall thickness). It serves the additional role of clamping the two sections of beam-pipe rigidly together (clamps at *z* about ± 15 cm) so that the critical inner cylindrical section of beam-pipe of length 12 cm and radius 14 mm can be made extremely thin: 0.25 mm wall thickness beryllium is considered possible.

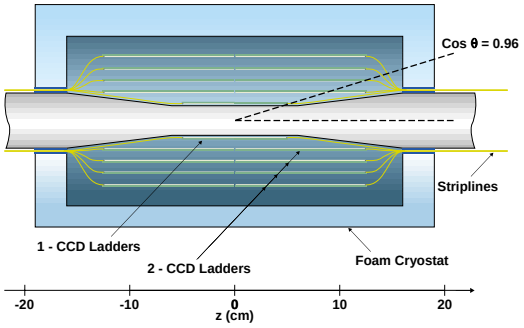


Figure 2: Cross-section of vertex detector. Cylindrical support shell linking the beam-pipe at $|z|\approx15$ cm is not shown.

Striplines and optical fibres are routed along the beam-pipe below the polar angle range used for tracking, connecting to inner electronics mounted in the form of a thin shell on the outer surface of the SR mask assembly.

For TESLA, the fast readout will necessitate fast collection of the signal charge. Relatively high resistivity material, depleted all the way to the edge of the epitaxial layer, will be used. The p^+ substrate is mostly removed by mechanical lapping and chemical etching, leaving a thin residual p^+ layer. The epi-layer thickness is current envisaged to be 20-30 μm, and the overall detector thickness about 60 μm. This architecture will ensure fast collection of the minimum-ionizing particle signal into the CCD buried channel about 1 μm below the surface.

Due to the Lorentz angle in the 4T field, the stored signal is dispersed 'horizontally' (across the CCD columns in $r\phi$ direction). Despite the 'vertical' clocking (in *z* direction) at 50 MHz, phasing of the clocks with the TESLA bunch crossings is expected to result in negligible vertical dispersion of the signal charge. Detailed optimisation of the pixel dimensions will depend on full 3-D simulation of the charge generation, storage and transfer to the edge of the CCD, but it is expected that optimised values (H and V) will lie in the range 20-30 μm.

As shown in Figures 2 and 3, the thin CCDs in layers 1-3 comprise all the material in the fiducial volume out to $|\cos\theta|$ = 0.96, used for high precision tracking for vertex

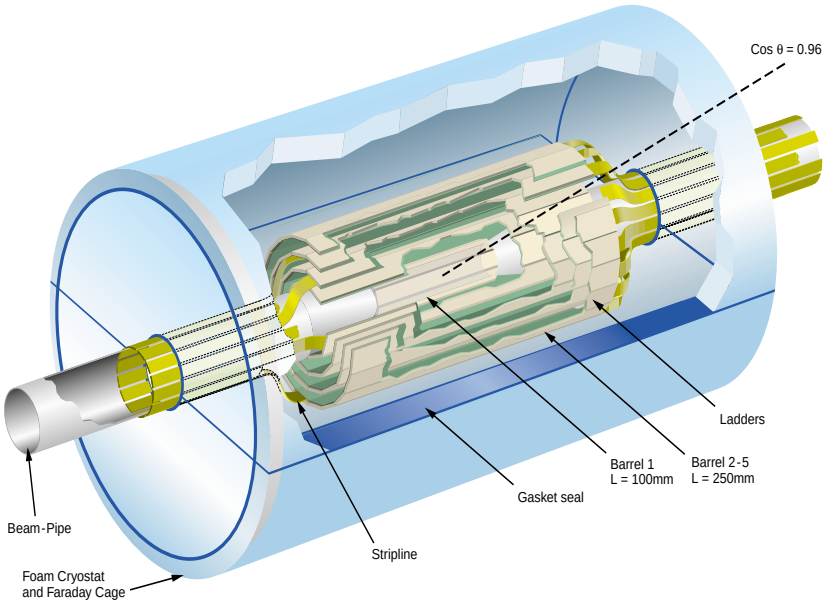


Figure 3: Isometric view of the vertex detector, again without showing the support shell

reconstruction. Beyond this volume, material is less critical and one can afford mechanical supports and readout electronics. This approach illustrates both the strengths and weaknesses of the CCD design. The advantage is unprecedented quality of impact parameter measurement over the maximum polar angle range, due to the minimal material and heat load, allowing the critical volume to be cooled by a gentle flow of nitrogen gas. The disadvantage is the requirement to transfer the signal charge packets out of the fiducial volume before they can be sensed. The innermost layer consists of single-CCD ladders, read out from both ends, while layers 2-5 are made of 2-CCD ladders, joined by a thin silicon bridge and read out from the outer ends only. Thus in some cases signals of only about 1000 electrons have to be transferred faithfully over a distance of up to 12.5 cm (~ 6000 pixels) en route to the CCD output. While this is a standard procedure for scientific grade devices, achieving this at high speed and in a non-negligible radiation environment is challenging.

All the thin ladders are stabilised mechanically by being bonded to 'ladder blocks' which are able to slide along rigidly supported 'annulus blocks', the ladders being pinned at one end and held under tension by springs at the other (sliding) end as shown in Figure 5. This support system extends the

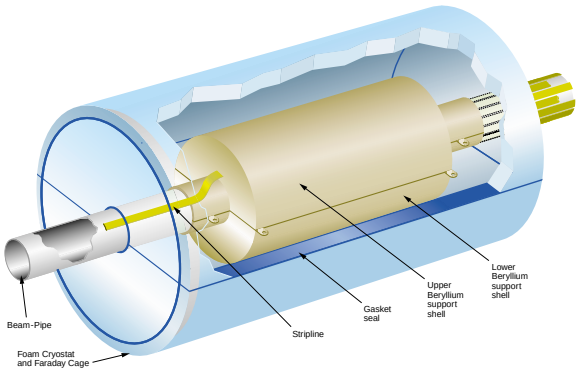


Figure 4: Beryllium shell which supports the 5 detector layers and provides stress relief to the delicate inner section of beam-pipe.

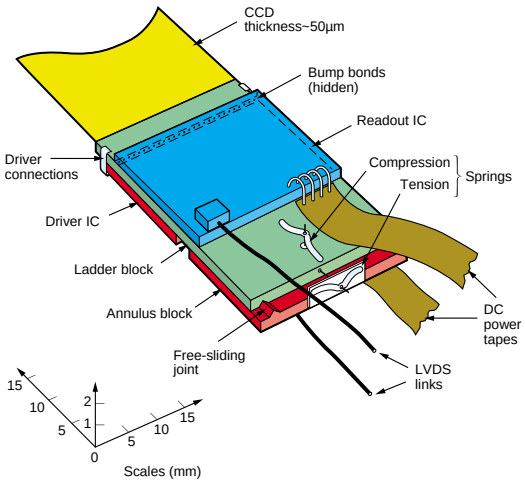


Figure 5: Layout of components at end of ladder. The compression spring establishes correct engagement between the blocks, while the tensioning spring stabilises the shape of the ladder.

Layer	Radius	CCD L×W	CCD size	Ladders and CCDs/lddr	Row clock fcy and Readout time	Bgd occupancy	Integrated bgd
	mm	mm^2	Mpix			Hits/mm^2	kHits/ Train
1	15	100×13	3.3	8/1	50 MHz/50 μs	4.3	761
2	26	125×22	6.9	8/2	25 MHz/250 μs	2.4	367
3	37	125×22	6.9	12/2	25 MHz/250 μs	0.6	141
4	48	125×22	6.9	16/2	25 MHz/250 μs	0.1	28
5	60	125×22	6.9	20/2	25 MHz/250 μs	0.1	28

Table 1: Key parameters of the TESLA vertex detector design. Background occupancy is based on calculated density per BX multiplied by number of BX during readout of that layer.

principles pioneered in the SLD vertex detectors [4,5], and is discussed in detail in Section 3.5. As well as providing the mechanical support for the CCD, each ladder block carries the local electronics components in the form of two or three integrated circuits. The driver chip (see Figure 5) generates the waveforms which shift the stored signals row by row down the device. The readout chip receives the analogue signals from all columns in parallel as they are shifted out of the active area to buffer amplifiers. This chip incorporates analogue-to-digital conversion, correlated double sampling to suppress reset noise in the charge-sensing circuit, data sparsification by a sequence of pixel- followed by cluster-comparators, and data storage.

Given that TESLA provides the more challenging accelerator environment, this option has been used for the detailed design study. The NLC situation is similar, but with much relaxed readout requirements. Parameters of the suggested TESLA detector (799 Mpixels) are listed in Table 1. Processed data stored in the readout ICs during the bunch train, amounting to ~ 8 Mbytes, are read out via a few optical fibres between trains. The power dissipation in the drive and readout ICs will considerably exceed the capability of gas cooling. In this region, the material budget is far less critical and one can consider a more robust cooling system, specifically evaporative nitrogen cooling as used successfully in the CCD vertex detector of the CERN NA32 experiment [2], the first particle physics experiment in which a pixel-based vertex detector was used.

The material budget is shown in Figure 6. The beam-pipe and critical first 3 layers amount to 0.25% X_0 at $\cos\theta = 0$ and rise to only 0.8% X_0 at $|\cos\theta| = 0.96$. The detector has 5-hit coverage to $|\cos\theta| = 0.9$, beyond which the end supports and electronics of layers 5 and 4 are encountered. The support shell and cryostat are beyond the region of high precision tracking. By the time the particles encounter this material, their impact parameters are well measured.

2.3 Generic detector performance

In this section, we discuss simulations based on the complete TESLA tracking system, namely the vertex detector, intermediate tracking detector (ITC) and main tracking detector (TPC) operating in a 4T solenoid field. Details of these studies are reported in [6].

The most important figure of merit for any pixel-based vertex detector can be expressed by the precision with which one measures the

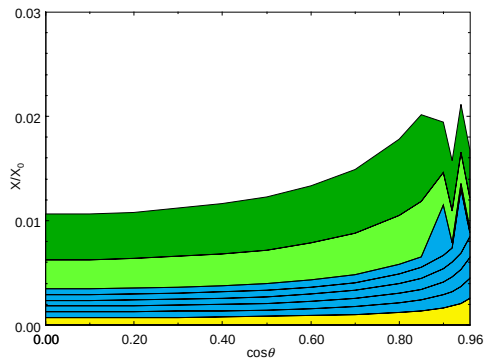


Figure 6: Material budget as function of polar angle (beam-pipe, each of 5 layers, support shell and cryostat)

track impact parameter to the IP, separately in the $r\phi$ and rz projections. For a set of cylindrical detectors, this resolution can be expressed as

$$\sigma = \sqrt{a^2 + \left(\frac{b}{p \sin^{\frac{3}{2}} \theta} \right)^2}$$

The constant a depends on the point resolution, layout and geometrical stability of the detectors and b represents the resolution degradation due to multiple scattering, which varies with track momentum p and polar angle θ. For the present detector design, the values of a and b are similar for both projections, and take the values 4.2 μm and 4.0 μm respectively. An example is plotted in Figure 7. These calculations are based on a full GEANT description of the TESLA detector, and use the BRAHMS detector simulation program.

The other important performance parameter is the 2-track resolution, which is particularly relevant to the core of high energy jets where the particles traverse the inner VTX layer. With a clean 2-track resolution in space of about 40 μm, CCDs are extremely robust. However, some Bs decay close to or beyond layer 1, giving merged or single-hit data in this layer. Experience from NA32 shows that these long-lived particles will form a particularly clean category, given unambiguous information from the outer layers. However, these questions need detailed study.

Studies of the physics performance of such a detector system are just beginning.

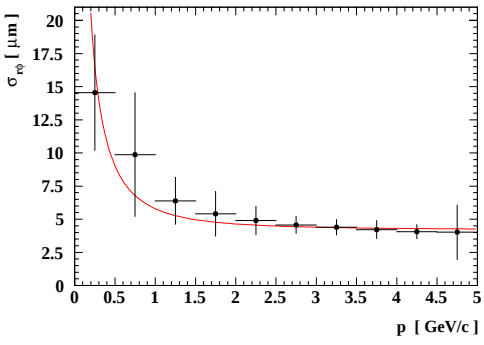


Figure 7: Track impact parameter resolution in $r\phi$ vs momentum for $\theta = 90^{\circ}$, for 4T solenoid field

First results are reported in [6]. As an example, the capability for b and charm tagging for $Z \to q\bar{q}$ is shown in Figure 8. Such events are a widely used benchmark for vertex detectors, and the 45 GeV jets are representative of the high multiplicity events in the TeV regime. In fact, the energy dependence of the flavour ID is not large. For b tagging, one finds only a modest improvement with respect to the SLD vertex detector, which was already close to optimal. However, there is a dramatic improvement in the charm tagging performance. The figure also shows the charm performance in the case of predominantly b background, which is relevant to the important physics example of measuring Higgs branching ratios. The performance for even more delicate physics requirements such as vertex charge and charge dipole determination have still to be studied. However, from SLD experience, one can be confident that clean measurements of these quantities will provide extremely powerful physics tools. In general, a detector with these performance specifications should upgrade most measurements almost to the asymptotic level for extracting physics, as has already been achieved in the simplest case (b tagging) at SLD.

3 R&D programme since October 1998

3.1 CCD assemblies

At the time of the original proposal, before the need for untriggered operation was established, it was already clear that readout speeds about 10 times faster than at SLD

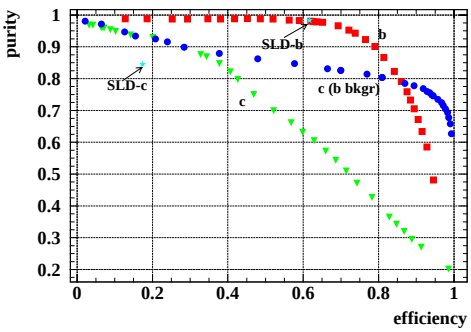


Figure 8: b and charm tagging efficiency/purity performance compared with the best existing detector.

would be needed. The CCD58 from Marconi was selected as having an output register with proven capability to operate at 50 MHz. For R&D purposes, it is desirable to have access to the drive and readout electronics, so it was decided to mount the CCD on a motherboard with bundles of cables providing matched low impedance drive signals from electronic modules outside the test cryostat. The CCD output signals are connected to buffer amplifiers on the motherboards, with 50 Ω coax connections to external processing electronics. These assemblies will provide ideal structures with which to test the limits of high speed register clocking and readout with bandwidth exceeding even the TESLA requirements.

To date, two of these assemblies have been completed, with somewhat different designs of external cabling. Once tests have established their performance characteristics, further assemblies will be produced for use in the Liverpool and RAL test facilities.

3.2 Test cryostats

The CCD assemblies will be operated in temperature-controlled cryostats. That at RAL has been commissioned, provides for operation down to about 120 K, and now has one of the CCD assemblies installed and undergoing initial testing, as shown in Figure 9. The cryostat at Liverpool University is specially designed using liquid helium to operate to much lower temperatures, of particular interest for radiation damage studies. It has been designed and built in the Liverpool workshops, where there is wide experience of making cryogenic systems, and is currently being commissioned. One of its special features is the possibility of laser illumination of the CCD, which will be valuable for quantitative studies of radiation effects.

3.3 Readout and drive electronics

The high current drive electronics and the analogue-bias modules were designed by Richard Stephenson's group in the RAL Instrumentation Department (ID), which has had long experience with electronics design

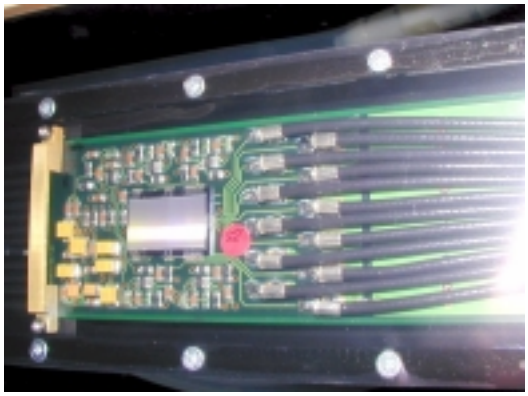


Figure 9: Photograph of CCD58 mounted on its motherboard and installed in the test cryostat. CCD dimensions are 12.2×23.2 mm^2.

for CCD vertex detectors. Most of the equipment is delivered and operational, with the final VME modules due within the next few months.

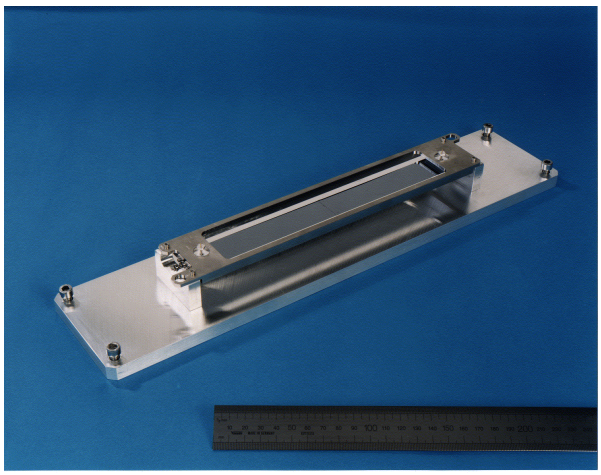
For the sequencing logic, the ADCs and digital processing, the most economical solution was to join the customers for the VME generic modules being designed by the ESD group in ID. Due to staff losses of some key people (the usual problem of CLRC salaries not competing with industry) these modules are seriously delayed. However, it has been possible to borrow sequencers and ADCs from LHC groups which will provide partial high-speed readout capability in the near future (next month or so). The complete interim VME system is now being commissioned at RAL.

3.4 Test system results

To date, it has been possible to test the four 3-stage output circuits on the CCD58 shown in Figure 9, which show correct gain and plausible noise reduction on cooling. Serious study of the CCD system clocked at various rates up to 50 MHz will begin next month. The full readout using the generic modules will become available in the summer. At that time, the duplicate system for use at Liverpool will be completed.

3.5 Mechanical R&D programme

At the time of the original proposal, it was clear that the more ambitious physics aims depended on reducing the layer thickness well



(a)

(b)

Figure 10: (a) Photograph of mechanical prototype of a 2-CCD silicon ladder of thickness 60 μm and length 25 cm, with (b) details of the spring tensioning system at one end.

below the figure of 0.4% X_0 achieved for the SLD detector (which was already a record). The proposal was to thin the CCDs close to the epitaxial edge (30 μm) and make a firm attachment to a beryllium substrate, building on the technology developed by Marconi for back-illuminated CCDs for astronomy. Stresses due to differential contraction were calculated to limit the thickness of such assemblies to at best 0.12% X_0. Subsequently, we looked into the rapidly evolving technology for paper-thin-packages (PTPs) and learned that modern procedures might permit the use of unsupported silicon ladders of thickness ~ 60 μm. Considering first layer 1, the single CCD would be attached with adhesive to ceramic 'ladder blocks' at each end, these blocks being assembled onto matching 'annulus blocks' in the detector support shell, as shown in Figure 5. The ladder blocks would be pinned at one end, and free to slide at the other. This general design follows that employed in SLD, where the sliding ends were required to compensate for differential contraction between the ladders and support shell. The difference in the case of the unsupported silicon ladders is that the CCDs would be tensioned by springs at the sliding end, gaining their mechanical stability in this way, somewhat analogous to the wires in a drift chamber, rather than due to their intrinsic stiffness. For the outer layers, the two CCDs would make a butt joint, linked by a thin silicon bridge. The advantage of the thin silicon option is a layer thickness of about 0.06% X_0 which, as shown in Section 2.3, results in a very favourable multiple scattering term in the impact parameter formula.

The R&D programme to prove this new design concept is proceeding in two main stages. For the first, 2-CCD mechanical prototypes are assembled with unprocessed silicon rectangles of dimensions 125×20 mm each, of thickness 60 μm, as seen in Figure 10. The assembly is clamped to a coordinate measuring machine (CMM) and the sagitta measured. This measurement is repeated 100 times, releasing the spring tension so the ladder visibly sags between each measurement. The standard deviation on the sagitta plotted in Figure 11 indicates that

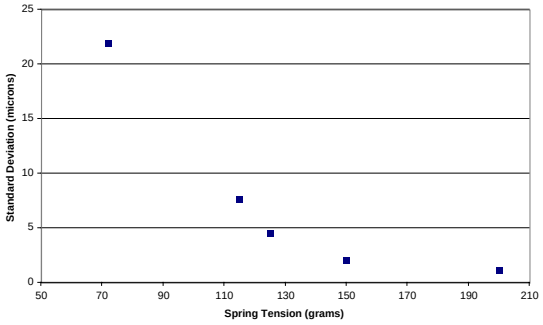


Figure 11: Sagitta stability as function of tension applied to the unsupported silicon.

for a spring tension above 150 g the mechanical stability at the centre of the ladder is better than 3 μm .

This result, while extremely encouraging, is only the first step. Plans for the future programme are outlined in Section 4.7. It should be noted that this approach to the mechanical design may be optimal for LC vertex detector technologies other than CCDs as long as the in-detector power dissipation is small. On the other hand, higher power dissipation would necessitate a robust and hence massive cooling system, as for example for hybrid pixel detectors as used for LHC. Such systems should be avoided if possible because of the degraded measurement of low momentum tracks, and hence of physics performance.

The measurements have so far been made by borrowing time on the ATLAS SmartScope system at RAL. Once the cryogenic survey system is running smoothly, it will be transferred to Oxford, where a white light interferometric system has been prepared for dedicated use by the LCFI collaboration.

4. Future R&D Programme

The achievements of the past two and a half years can be summarised under the following headings:

- defining the problem
- building up experimental facilities
- building up manpower.

Unless there are some radically new developments, it appears that the problem is now rather well defined. Members of the LCFI collaboration will of course continue to play a strong role in the physics studies, where there are very many open questions. However, these studies are unlikely to alter the goals for the detector designer. The last major changes took place at the Frascati ECFA/DESY workshop in November 1998, and at the CERN 'Detector Concept' meeting in July 1999. At Frascati, it became apparent that the subtle signatures for SUSY and other possible new physics precluded triggered operation. This had significant implications for all possible vertex detector options. At the CERN meeting, it was shown that the worst-case background at 4T would permit an inner layer coverage to $|\cos\theta| = 0.96$.

With the experimental facilities and manpower in place and the problems defined, the collaboration is now seriously engaged in finding the solution. To put things in perspective, it has to be said that this solution is not yet well-defined and may not be unique. Other groups are exploring other options (PN CCDs, CMOS and DEPFET pixel devices and hybrid pixel devices). The option being pursued by our collaboration (MOS CCDs) is based on the firm foundation of the two highest performance vertex detectors yet built, operating in the world's first LC environment. However, the requirements for the future LC are more challenging, and the CCD technology could fail, particularly if it is not supported by a substantial R&D programme. Even if successful, it could be overtaken by an alternative approach. Given the cost of the future LC and the essential role of the VTX in accessing the physics, we consider it an obligation on the part of the world-wide detector physics community to push hard on all options. In the event that more than one approach is successful, the LC community will be in the fortunate position of being able to choose between two winners.

The LCFI collaboration therefore proposes to focus its efforts over the next 4-6 years on establishing whether the CCD technology can be extended to meet the requirements for the LC vertex detector. The proposed R&D programme will use the experimental facilities that have been built up over the past two years in the universities and at RAL, and will pursue all aspects in parallel (7 work packages discussed in Sections 4.1 to 4.7). The rationale for this approach is that while individual problems may be soluble separately, the most challenging will probably be in the *system integration*. This view is based on the 6-year R&D programme for the SLD vertex detector (1984-1990), where a system approach led to the early discovery and eventual solution of inter-system problems such as various effects of differential

contraction and micro-connectors, which would have been much more serious had they emerged late in the programme.

Since the need for untriggered operation imposed the requirement of column-parallel CCD architecture, the detector design has advanced to a fairly detailed conceptual level, as was discussed in Section 2. The work packages described in the next 7 sub-sections will establish whether such a conceptual design can in practice be realised. This work will be a close collaboration between the physicists and engineers of the LCFI collaboration, engineers of the Instrumentation Department at RAL, some of whom have long experience with CCD vertex detectors, and the scientists and engineers in the CCD department at Marconi Applied Technologies, who again have been close collaborators on a series of successful vertex detector projects since 1979.

4.1 CCD design and simulations

The column-parallel architecture has a number of advantages with respect to the standard serialised layout. These are the speed potential (obligatory for TESLA, valuable for NLC), convenience of local 2-D cluster processing and data sparsification, and minimal cable plant from the detector. Since the cables necessarily lie in the volume for forward tracking and calorimetry, this is a major advantage. For these reasons, it is proposed to focus the R&D programme exclusively on this architecture. To pursue other options in parallel would require an expanded R&D capability.

The column-parallel CCD design is intrinsically simple, since the readout register is omitted. The maximal degree of parallelism has the highest possible speed potential. This architecture has been used with much larger pixels (not useful for vertex detectors) in PN CCDs. However, for MOS CCDs with small pixels, the development of sub-micron CMOS processing is the key to the realisation of this approach, which could have numerous application areas. Staggering of the bump bonds linking the CCD to the readout chip, shown in Figure 12 and 13, establishes compatibility between the column pitch of

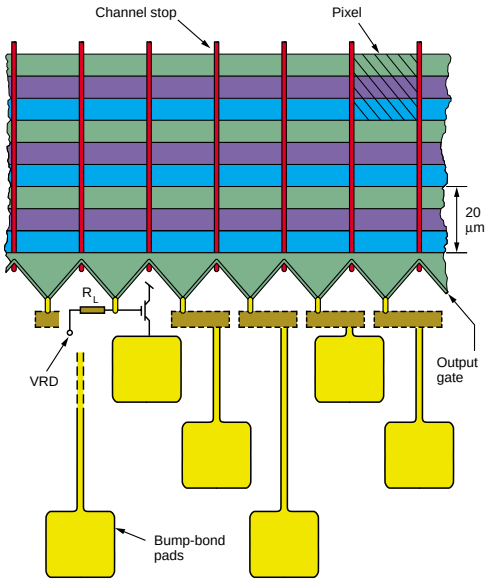


Figure 12: Edge of column parallel CCD in region of interface to readout chips.

(probably) 20 μm and the minimal spacing between bump bonds of approximately 30 μm with current technology. There is one apparent disadvantage in the column parallel approach with respect to the serialised output, which is the lack of automatic gain equalisation between the transverse (column-to-column) cluster data, and hence possible systematic effects in the inferred $r\phi$ track position. Such effects will be much smaller than in the active pixel sensor (APS) approach, and should lend themselves to simple calibration procedures.

The complexity of the column-parallel design advances progressively from the NLC to the TESLA requirements as indicated in Figure 14. For the former, the factor 30 increase in speed relative to SLD can be achieved with standard CCD processing and

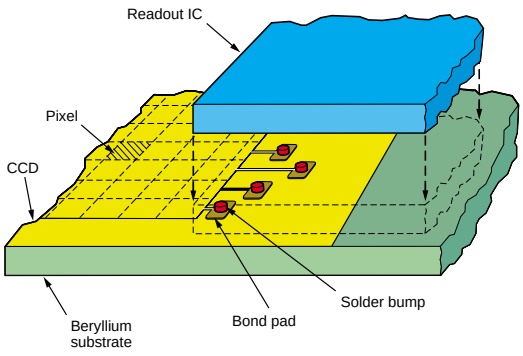


Figure 13: Exploded isometric view of the interconnect region between CCD and readout chip.

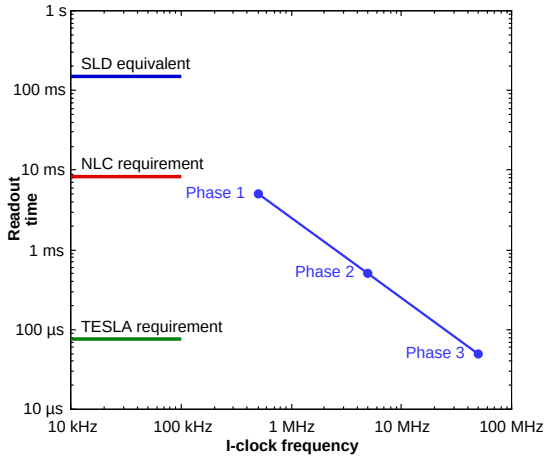


Figure 14: Readout time vs I-clock frequency (frequency of clocking imaging area) for a CCD of length 10 cm. For column parallel operation, Phase 1 can be achieved with standard processing, where Phase 3 will require reduced resistances and reduced gate voltages.

clock voltages. In this case, the main challenge is the design and production of the output circuits on a pitch of 20 μm, capable of driving the bump-bonded preamp input to the readout IC. The Marconi design team have already looked informally at the problem and succeeded in producing a 2-stage layout having a bandwidth close to 50 MHz, driving a 4 pF load (Figure 15). The power dissipation in the second stage would be excessive, but it appears that an effective load capacitance of only 60-80 fF may be realistic for a bump-bonded readout chip, so a single-stage source follower should suffice even at 50 MHz. Once the project is approved, a serious collaborative effort between the CCD design group and the RAL microelectronics design group can begin; there is every reason to expect a positive outcome. V. Radeka has looked into the potential noise performance, with very favourable preliminary conclusions.

The speed increase by an additional factor 100 to achieve the TESLA goals raises many problems. It is proposed to tackle these in two further steps, each aimed at a factor 10 in clocking speed. A preliminary study using PSPICE by our collaboration [7] has shown the way forward. As an example, the simulated clock waveforms for one of two phases operating at 50 MHz are shown in Figure 16 at various extreme locations of a layer 1 CCD. If waveforms of this quality can be realised in practice, there will be no problem in achieving excellent charge transfer efficiency (CTE) at this frequency. It therefore appears that 50 MHz operation of a layer 1 CCD will be achievable, subject to the following conditions:

- full depletion of the epitaxial layer, for prompt charge collection
- 2-phase operation, sinusoidal clocks
- partial metallisation of the imaging gates, for reduced resistance
- extended clock buslines, probably mostly on top of the polyimide passivation layer
- gate voltages in the range 1-3 V, for acceptable power dissipation

While these conditions are necessary, experimental work will be needed to find out if they are achievable. Furthermore, they are not in themselves sufficient. Reduced resistance increases the sensitivity to parasitic inductances in the CCD structure and in the connections between the driver IC (see

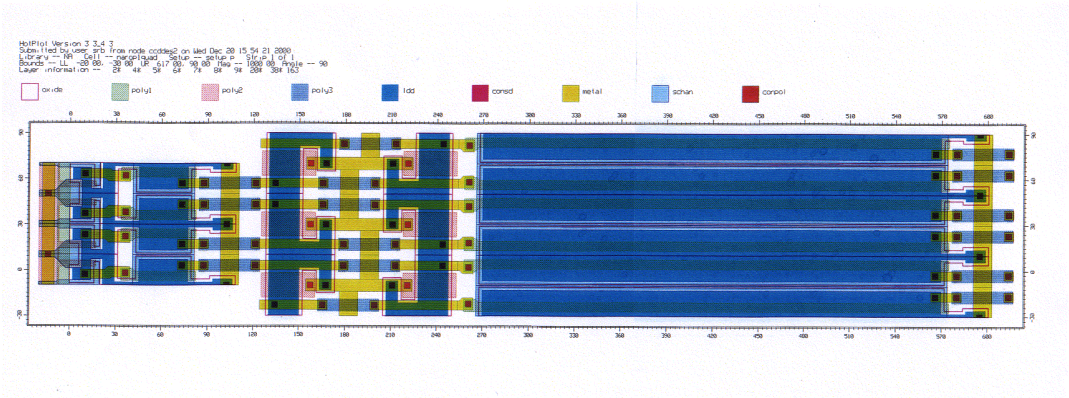


Figure 15: Possible 2-stage output circuits on a pitch of 20 μm ; input on the left, second stage output on the right.

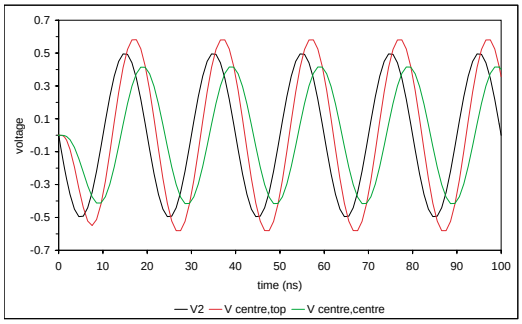


Figure 16: 1 phase of 2-phase clock waveforms at extreme positions of the CCD imaging area, for a layer 1 CCD operated at 50 MHz.

Section 4.4) and the CCD. Full depletion increases the magnitude of charge smearing due to $\boldsymbol{E}\times\boldsymbol{B}$ effects. 50 MHz clocking will be challenging in terms of the details of the potential wells in the imaging area (potential pockets which can degrade the charge transfer efficiency). On the other hand, optimal shaping of the gate electrodes can enhance the speed capability. The question of reduced gate voltages will become of paramount importance by the third phase of the programme. Ideas for achieving this include low-level implants and even a no-implant option using variable dielectric thickness or other structures to create the potential wells. Whether these can be made stably and with sufficient radiation resistance remains an open question. There are reasons for optimism, since the signal charges to be stored are almost entirely below 10^4 electrons, a fortunate consequence of the well-defined LC backgrounds, all coming from minimum-ionizing particles.

All these issues would be extremely painful and expensive to investigate experimentally. A full 3-D simulation of the minimum-ionizing particle charge generation, collection into the buried channel and transfer is needed. Such details as the phasing of the fast clocks with the bunch crossings will become important, in the case of TESLA. As a result of our funded proposal in 1998, it was possible to purchase the powerful ISE-TCAD software, which is installed and in use at Liverpool University. The challenging CCD architecture has not yet been modelled, but this will begin when a full time physicist to work on device modelling is recruited. At RAL, the Instrumentation Department has recently created a semiconductor devices modelling group, and we are requesting funds for them to work on this project, using the already-installed Davinci software. Between these two groups, it should be possible to provide Marconi with the necessary input for the CCD design, and so minimise the number of test structures to be made. There is every reason to be confident in this collaborative approach, which has been followed over many years by the Leicester X-ray astronomy group working with Marconi. A number of major CCD innovations have emerged from their studies.

4.2 CCD experimental studies

Marconi will manufacture test structures and prototype devices for each of the 3 phases of the project. These will be included in batches used for standard production, so the processing costs will be modest. What would be much more expensive would be to ask Marconi to carry out detailed evaluation of these devices and structures. Instead, the plan (which worked well in the case of the SLD CCD development and production) will be for the LCFI group to in general take delivery of untested devices. With the flexible test facilities built up at RAL and Liverpool University from the first two years of funding to our collaboration, we are well placed to make the necessary measurements. Highly skilled staff are now available (some new, some coming free from LHC R&D programmes) to undertake these studies. The test equipment permits electrical and opto-electrical investigations over a wide range of temperatures, fully representative of the vertex detector operating conditions. For more sophisticated studies, the comprehensive facilities now under construction at Liverpool University's Semiconductor Detector Development Centre (funded from their JIF award) will be extremely useful. In addition, one or two of the expert CCD design/test engineers at Marconi will participate in these investigations, using their own sophisticated test equipment.

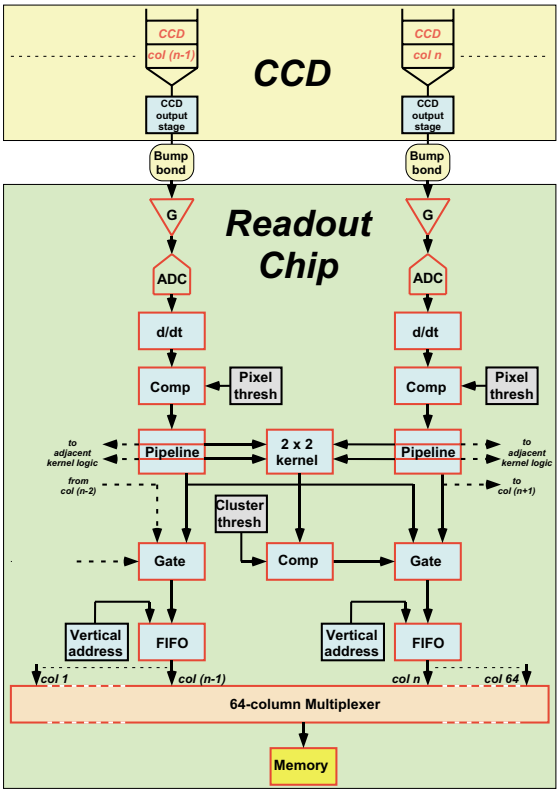


Figure 17: Preliminary logic of readout integrated circuit.

4.3 Readout IC

As already mentioned, the first requirement is for high density interconnects (bump bonds) between the CCD output and the preamp inputs as shown in Figures 12 and 13. Based on the technology used for hybrid pixel devices, these connections can be made routinely and reliably [8]. However, they do impose several important boundary conditions on the plans for ladder assembly (processing temperatures etc). The first approximation to the logic on the readout chip is shown in Figure 17.

There are a number of options for the circuit between the CCD output gate (effectively a high impedance current source which injects the signal charge onto the next stage) and the ADC input. One possibility is a single-stage source follower on the CCD and a voltage sensing preamplifier on the readout IC, but a detailed analysis of the noise performance of this and other options needs to be undertaken. It may well suffice to make AC coupled connections from the CCD, so that the staircase of signal steps along a column is converted to a series of pulses with few μs decay time. The potential node reset noise may be avoided by carrying out the reset operation only between bunch trains. With this approach, a 4- or possibly 6-bit ADC will suffice. The difference between successive ADC values is used to measure the signal content of each pixel, and these are fed to a comparator with a pixel threshold set to about twice the RMS noise. This results in full efficiency for minimum-ionizing particle detection ($\gtrsim$ 99.9%) with a sufficiently low noise rate to be used by the next stage, where a 2×2 kernel is used to establish whether the overall cluster forms an acceptable minimum-ionizing particle candidate. If so, the address of a corner pixel and the contents of the 2×2 array are stored in a local memory. The optimal layout will probably be for the memory to be a separate chip, bump bonded to the ladder block behind the readout chip, the two chips being interconnected by metal traces on the ladder block. Finally, the stored data are transferred to one of the bunch-train data processors via an optical link.

As with the CCDs, the readout chip will be developed in three stages, designed to operate at 0.5 MHz, 5 MHz and 50 MHz. Achieving the required noise performance will be much easier for the first phase devices, and challenging for the third. However, ongoing advances in CCD design and submicron CMOS design give good reasons for optimism that even the most demanding performance requirements can be met. The prognosis is complicated by the issue of clock feedthrough which has always played a large part in the noise performance of CCDs. For the conventional architecture, these effects have been well controlled up to 10 MHz clocking frequency. For the column-parallel architecture, the much greater CCD capacitance will be a complication, but the balanced sinusoidal 2-phase drive will help. If the clock voltages can be drastically reduced, this will be of further assistance. This is one example where the system aspects are difficult to predict, and where detailed experimentation at each of the three phases of the programme will be essential.

4.4 Driver IC

The driver requirements for the first phase of the programme will be conventional, with current experience a clear guide that inductive effects are easily controlled. By the third phase, on-CCD power dissipation requires that the problems of operation with reduced gate voltages should have been solved. If so, the design of the driver IC will be considerably simplified. The technology developed for numerous compact RF generation systems may well be applicable. Commercially available ICs, as used for the current R&D programme, will be perfectly adequate for the initial studies.

By comparison with serialised CCD readout, where the drive waveforms must preserve the integrity of the stored signals from the very beginning of the R drive pulse train, the possibility to start the column-parallel clocking shortly before each pulse train means that the pattern of waveforms has time to settle down over the entire imaging area before the arrival of the first signal charges, and to continue to run stably till the last signals have been transferred to the output circuit and onto the readout chip. Operation of the CCDs in a 'pulsed power' mode (clocked for only 1 ms every 200 ms) is therefore guaranteed to be acceptable, with a huge reduction in the average power dissipation.

4.5 Radiation effects

In one sense, the plans have changed little with respect to the proposal approved in 1998. The test facilities at Liverpool University will be completed within the next few months, and these will permit a comprehensive study of radiation effects in CCDs over a wide range of temperatures and other operating conditions. There remain discrepancies in the published data, particularly with respect to neutron damage, and these will be studied comprehensively.

However, the column parallel architecture changes the picture significantly. The fast clocking will reduce the loss of CTE since traps, once filled, will have less time to become emptied before the arrival of the next charge packet. Furthermore, the use of a higher resistivity *n* implant (adequate for smaller well capacity) will reduce the phosphorus concentration, and hence the generation of E-centres. Against this, the goal (in phase 3) of reduced clock voltages may increase the sensitivity to voltage shifts due to ionising radiation. Radiation effects including single event upsets (SEUs) in the readout chip may be an issue, though this is less likely due to the much lower hadronic background than at LHC.

The general impression is that the radiation hardness of the detector systems envisaged are likely to be improved with respect to the conventional CCD architecture. However, this is by no means certain and the picture could change through the three-phase R&D programme. This aspect of the detector development will need to be followed carefully. There are at every stage options for radiation hardening of either the CCD or the readout chip, but these should be pursued only if they prove necessary. At SLD, initial concerns about possibly fatal neutron levels proved to be exaggerated, and CCDs processed with the most radiation-soft technology worked reliably with only minor changes in operating parameters throughout the life of the experiment.

4.6 System electronics

As discussed in Section 3.3, the test facilities approved in 1998 are largely in place. The main missing elements are 'generic modules', VME modules which will be used for extremely flexible control of the drive and readout of CCDs at frequencies up to 50 MHz, the maximum envisaged for this project (and 10 times faster than used for SLD). While the generic modules are being designed and built by the Electronics Systems Design (ESD) Group, the local drive and analogue-bias modules from the Electrical and Control Design (ECD) Group are being augmented by digital sequencer and ADC modules borrowed from LHC projects. A fast CCD (CCD58 from Marconi) has been mounted on a motherboard which is fitted into a test cryostat, as shown in Figure 9. This system feeds drive pulses down bundles of

fine coax cable, providing relatively low impedance signals capable of driving a CCD readout register at 50 MHz. This system will be used for studies with fast readout of devices with standard architecture, from which it will be possible to learn many valuable lessons for the column parallel design, particularly regarding the output circuit. The system will also be useful for studies of custom CCDs and other test structures from Marconi as the column parallel project advances. However, it will need to be progressively upgraded and developed particularly for phases 2 and 3 of the project. For this reason, the ongoing participation of the ECD group will be essential. On the current planning, the delivery of the powerful generic modules will complete the support required from the ESD group for this project.

4.7 Mechanics and cryogenics

As discussed in Section 3.5, the R&D for the unsupported silicon ladders has made an encouraging start. The next step will be to check the stability when cold. For such measurements, a special survey cryostat similar to, but larger than that used on SLD has been constructed and commissioned. Measurements are made through a double glazed window, evacuated between the glass panes, and with the lower surface of the outer pane coated with a thin layer of gold and heated electrically to prevent condensation. The main concerns with low temperature operation would be stiction effects and lateral distortions due to stresses between the ladder and ladder blocks. These studies are about to begin. Figure 18 shows the survey cryostat mounted on the CMM for the first time.

Figure 18: Survey cryostat with its cooling system mounted on the SmartScope CMM for the first measurements of temperature dependence of the shapes of stretched-silicon ladders.

Once the delicate procedures for thin ladder assembly, handling and measurement are under control, and the selection of adhesives and other materials have been proven over a wide range of temperature, the silicon will be changed from unprocessed to CCD-processed material. We have taken delivery of such samples from Marconi, in the form of thick-thin sandwiches attached together by wax. It is believed that the present system of jigs, assembly tooling and procedures will be applicable with minor variations to these samples. The processed silicon when unsupported takes on a high degree of concave curvature. It is believed that it should pull straight with little force, so it may be stable with the tensioning system as developed. However, there will be more risk of problems related to differential contraction in such an assembly, so it will be important to test it thoroughly.

As well as the studies on single static assemblies, it will later be necessary to extend to dynamically cooled multiple-ladder systems. The most severe power dissipation conditions apply to the TESLA option. The PSPICE simulations referred to in Section 4.1 lead to a whole-detector power dissipation of only about 10 W if the goal of 1 V clocks can be achieved. This is even less than in SLD, and would easily lend itself to cooling of the ladders by a gentle flow of nitrogen gas. Even so, the thin stretched ladders will be inclined to vibrate. Simulations and tests will be done to establish whether this is a problem.

Apart from the ladders, there will be much greater power dissipation in the local driver and readout ICs. Since they are located outside the volume which is of importance for impact parameter measurement, they can be cooled more robustly. Evaporative nitrogen cooling as used on the NA32 vertex detector [2] appears to provide a promising solution, but careful prototyping, particularly with respect to induced mechanical vibration, needs to be carried out.

5 Conclusions

International progress towards the future linear collider is advancing rapidly. A huge investment in various options for the accelerator design is coming to fruition, with already one which is clearly viable for the next step to around 1 TeV. The UK (albeit mostly with US DOE financial support) had led the design and production of the highest performance vertex detectors yet developed, using CCDs from Marconi Applied Technology. For the new energy regime, extremely high performance vertex detectors will be required for precision measurements as well as for particle searches and other new physics. It appears likely that the MOS CCD architecture can be developed to provide the highest performance vertex detector option for the NLC and possibly also for TESLA. Even if the full performance goals for TESLA were to prove beyond reach, CCDs might still prove to be the best available technology. In any case, whether the development stops at Phase 2 or is able to progress all the way to Phase 3, the prospects for CCDs of length 10 cm being read out within 5 ms, 500 μs or 50 μs will all represent advances of great importance to other application areas.

The budget request for this 4-year R&D programme is detailed in Appendix D. We would like to emphasise that this programme is vital if the UK is to retain its world-leading position in this technology for the high-profile international LC, wherever and whenever built. We are fortunate in having the right combination of intellectual leadership in the academic, research and manufacturing sectors, all of whom are involved in this proposal. Without sufficient support, the entire R&D in LC vertex detectors will progressively pass to non-UK groups. It would then be very difficult, and very expensive, for the UK to regain its present position; it might also be difficult to retain the support for, or of, Marconi, with consequent significant loss to the UK technology base.

In principle, these developments could be supported by the Fundamental Technology Fund. However, it is not yet clear how this is going to be managed by EPSRC. The LCFI collaboration would much appreciate the advice of the Panel on this issue. In any case, we believe that it is essential that PPARC, advised by the Panel, strongly endorse the scientific and technical aims of this proposal.

References

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[2] CJS Damerell, Proc Physics in Collision IV, 1984 (Editions Frontieres) (1985) 453

[3] CK Bowdery and CJS Damerell, Workshop on Physics and Experiments with Linear Colliders, Waikoloa, Hawaii, World Scientific (1993) 773

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[5] K Abe et al, *Nucl Instr Meth* **A400** (1997) 287

[6] S Xella Hansen et al, LC-PHSM-2001-024 (DESY LC note)

[7] A R Gillman for the LCFI collaboration. Contribution to the Vertex 2000 workshop (Lake Michigan). To be published.

[8] O Ehrmann and J Wolf, Frauhofer IZM Berlin. Preliminary discussions.

Appendix A: Collaboration publications since October 1998

Ideas for a Vertex Detector at the Future e^+e^- Linear Collider.
CJS Damerell for the LCFI Collaboration.
Nucl Instr and Methods **A435** (1999) 16.

A TESLA-Compatible Vertex Detector Design.
T Greenshaw, for the LCFI Collaboration.
Physics and Experiments with Future Linear e^+e^- Colliders.
University of Barcelona publication (2000) 901.

A CCD Vertex Detector for a High Energy Linear e^+e^- Collider.
P Burrows, for the LCFI Collaboration.
Nucl Instr and Methods **A447** (2000) 194.

A Fast CCD Vertex Detector for the Future Linear Collider: Some Recent Developments.
A Gillman for the LCFI Collaboration.
Vertex 2000 Conference, Michigan 2000 (to be published).

A CCD Vertex Detector for the future Linear Collider.
T Greenshaw for the LCFI Collaboration.
Proc IEEE 2000 Conference, Lyon (2000) (to be published).

A CCD Vertex Detector for the future Linear Collider.
CJS Damerell for the LCFI Collaboration.
Proc LCWS 2000 Workshop, Fermilab (2000) (to be published).

Flavour tagging studies for the future Linear Collider.
S Xella Hansen et al.
Proc LCWS 2000 Workshop, Fermilab (2000) (to be published).

A CCD-based vertex detector for TESLA.
CJS Damerell for the LCFI Collaboration.
LC-DET-2001-023 DESY Linear Collider Note (2001).

Flavour tagging studies for the TESLA linear collider.
S Xella Hansen et al.
LC-PHSM-2001-024 DESY Linear Collider Note (2001).

Appendix B: Conference talks since October 1998

Ideas for a Vertex Detector at the Future e^+e^- Linear Collider.
CJS Damerell, Vertex 98 Workshop, Santorini, Greece

A TESLA-Compatible Vertex Detector Design.
T Greenshaw, LCWS 99 Workshop, Sitges, Spain

A CCD Vertex Detector for a High Energy Linear e^+e^- Collider.
P Burrows, Vertex 99 Workshop, Texel, Netherlands

A Fast CCD Vertex Detector for the Future Linear Collider: Some Recent Developments.
A Gillman, Vertex 2000 Workshop, Michigan, USA

A CCD Vertex Detector for the future Linear Collider.
T Greenshaw, IEEE 2000 conference, Lyon, France

A CCD Vertex Detector for the future Linear Collider.
CJS Damerell, LCWS 2000 conference, FNAL, Batavia, USA

Flavour tagging studies for the future Linear Collider.
S Xella Hansen, LCWS 2000 conference, FNAL, Batavia, USA

Appendix C: Collaboration participants

Institutes	Name	Category	% FTE on project					Comments
			01/2	02/3	03/4	04/5	Average	
Bristol	de Groot	ph	15	20	25	30	22	
	Foster	ph	5	5	10	10	7	
	RA	ph	25	25			12	2 year appointment
Glasgow	Bussey	ph	0	0	10	10	5	
Lancaster	Finch	ph	10	20	20	20	17	
	Sopczak	ph	15	30	30	30	26	
Liverpool	Biagi	ph	20	20	20	20	20	
	Carroll	ph	20	20	20	20	20	
	Casse	ph	30	30	30	30	30	
	Court	ph	20	20	20	20	20	
	Dainton	ph	10	10	10	10	10	
	Greenshaw	ph	10	10	10	10	10	
	Milstead	ph	10	10	10	10	10	
Oxford	Burrows	ph	30	40	(50)	(50)	17 (45)	Advanced Fellowship ends Feb 2003, continuation subject to future lectureship
	Christian	st	100	100			50	CASE student ends Sept 2002
	Devenish	ph	0	10	20	30	15	
	Myatt	ph	20	30			12	Retires Oct 2003
	White	ph	10	10			5	RA position ends Sept 2002
	Physicist	ph	(50)	(100)	(100)	(50)	(75)	Possible responsive RA
RAL	Burge	eng	5	5	5	5	5	
	Damerell	ph	100	100	100	50	87	Retires Nov 2004
	English	eng	20	20	20	20	20	
	French	eng	5	5	5	5	5	
	Gillman	ph	20	30	40	50	35	
	Johnson	app-ph	100	100	100	100	100	
	Lintern	eng	15	15	15	15	15	
	Manolopoulos	ph	20	20	20	20	20	
	Nichols	eng	5	5	5	5	5	
	Sankey	ph	20	30	40	50	35	
	Stefanov	ph	100	100	100	100	100	
	Stephenson	eng	5	5	5	5	5	
	Xella Hansen	ph	50	50	50	50	50	
	Physicist	ph	50	100	100	100	87	Future group leader

Note: Years on this table run from 1 April

Appendix D: Budget and manpower request

This request covers the 3-phase R&D programme, for which the time estimates are 12-18 months Phase 1, 12 months Phase 2, 12-18 months Phase 3, 4 years total.

For RAL, ID/ED manpower is converted from SY on the basis of 1 SY = £65K and identified by asterisks. PPD manpower is not listed.

Units are £K

	01/02	02/03	03/04	04/05	Total
Phase 1					
CCDs (design and M/F)	300				300
Bump bonding		147			147
Readout ICs	98*				98*
	48				48
Driver ICs	5				5
Phase 2					
CCDs (design and M/F		300			300
Bump bonding			147		147
Readout ICs		98*			98*
		40			40
Driver ICs		10			10
Phase 3					
CCDs (design and M/F)			150	150	300
Bump bonding				147	147
Readout ICs			98*		98*
			40		40
Driver ICs			20	20	40
Motherboard and external electronics (ECD)	65*	65*	65*	65*	260*
	15	15	15	15	60
External electronics (ESD)	49*				49*
	15				15
RAL-based detector simulations	33*	33*	33*	33*	132*
Thin ladder developments	18	18	18	18	72
Cooling system development	11	11	11	11	44
Mechanical/cryogenic design	13*	13*	13*	13*	52*
Totals	**670**	**750**	**610**	**472**	**2502**

The largest single element within the project are the three phases of the CCD design and development (£900K). Given the amount of work involved, this is in fact modest compared with the R&D for the SLD detectors VXD2/3. This probably arises from the fact that the goals of metal-buttressed poly, low voltage clocks and bump bonded outputs will all have spinoff for other customers. For this reason, Marconi are clearly absorbing part of the development costs.