# A CCD Vertex Detector For The Future Linear Collider

C J S Damerell

*Rutherford Appleton Laboratory, Chilton, Didcot, OX11 0QX, United Kingdom*

on behalf of the LCFI Collaboration

**Abstract.** The design work and R&D programme of the LCFI collaboration for a CCD vertex detector at the future linear collider is discussed. The physics goals can be met by a 5-layer cylindrical detector system of 800 Mpixels, with polar angle coverage to $|\cos\theta| = 0.96$. The main challenges are in the layer thickness and the readout architecture. The latter is particularly challenging for TESLA due to the time structure of the machine. Solutions to these problems are described and supported by simulations. Encouraging early R&D results on the question of layer thickness are reported. It seems probable that a well-supported 5-year R&D programme should lead to a buildable detector design which satisfies the physics goals.

## 1. INTRODUCTION

Since their invention 20 years ago, there have been many examples of the importance of vertex detectors in high energy physics. The UA1 top 'signal' at 40 GeV in 1984 could have been proved or disproved had the experiment been equipped with a vertex detector, as was pointed out at the time [1]. The eventual discovery of the top quark in 1995 owed a good deal to the pioneering vertex detector (the first at a hadron collider) of the CDF experiment. Had the LEP experiments not been constrained by their large beam-pipe, the evidence for a 115 GeV Higgs boson would now be conclusive, one way or the other. The ability of the SLD detector to produce world-leading physics results at the $Z^0$, despite having only about 2% of the LEP data, owed a lot to the small beam-pipe and high precision pixel-based vertex detector. Fortunately it will be possible to preserve this combination of small beam-pipe and very high performance vertex detector in the future LC, in contrast to the LHC where conditions for flavour identification remain rather unfavourable. These differences will lead to a high degree of complementarity between the physics capabilities of these two machines in the TeV regime.

The physics of interest includes standard model processes ($t\bar{t}$ production, high energy $W^+W^-$ production, etc) and (we hope) novel processes such as the production of supersymetric particles. Both classes of event lead to high multiplicities of heavy quark jets, for example:

$e^+e^- \to t\bar{t}$ (usually 6 jets, two *b*-flavoured and two *c*-flavoured)

$e^+e^- \to AH$ (12 jets, four *b*-flavoured)

Due to the low event rates for specific processes, and the need for precision measurements (eg of Higgs branching ratios) extremely pure and efficient *b* and *c* tags are necessary. In addition, the measurement of the vertex charge can distinguish *b* from $\bar{b}$ and *c* from $\bar{c}$. Even when the *b* quark hadronises into a neutral *B*, measurements of the charge dipole can be used. These techniques, pioneered in the topological vertex reconstruction of SLD [2], will be valuable in suppressing combinatorial background in multi-jet final states. Use of missing transverse momentum in reconstructed decay vertices, in conjunction with $\pi^0$ and $\eta^0$ reconstruction in highly segmented calorimeters, will permit some degree of compensation for missing neutrino energy in jets with semileptonic *B* and *D* decays.

In this paper, we review the current status and R&D plans for a CCD-based vertex detector for the future LC. While this is not the only candidate for a pixel-based system, it is firmly grounded in the successful SLD detector [3]. Whether advances in CCD technology will permit this architecture to retain its preferred status for this application, or whether it will be overtaken by other technologies, is an interesting question. Healthy competition is a valuable spur to developing at least one technology to match the physics challenges of the future LC.

## 2. DESIGN OVERVIEW

The first key to performance of a vertex detector is the beam-pipe radius. If the inner layer cannot be sufficiently close to the IP, multiple scattering will degrade the association of tracks to vertices, and hence the physics performance. In SLC, a major effort on masking design resulted in a beam-pipe radius of 24 mm, half that of LEP. At the future LC, great care has again been taken in the design of the collimation and final focus systems, so that figures in the range 10 to 14 mm are foreseen, affording an excellent opportunity to satisfy all the major physics goals.

A small-radius beam-pipe can be made thin, provided it can be protected from external stresses, particularly during installation. This can be achieved by enclosing the vertex detector in a rigid beryllium support shell which grips the beam-pipe at its robust large diameter sections, beyond the fragile, thin walled small diameter section which extends to $|\cos\theta| = 0.96$, as shown in Figure 1. This will allows an inner section of beam-pipe of wall thickness 0.25 mm beryllium (0.07% $X_0$).

The next challenge is to minimise the thickness of the detector layers. Following the evolution in SLD, where this was reduced from 1.1% $X_0$ (original detector) to 0.4% $X_0$ (upgrade detector) the goal is 0.06% $X_0$. Also, in order to achieve robust standalone tracking, a 5-layer geometry is considered. This detector would then contain 800 Mpixels of size $20 \times 20\ \mu m^2$, a realistic advance on the SLD detector of 307 Mpixels. The materials budget, indicated in Figure 2 is most critical through the beam-pipe and detector layers (0.37% $X_0$ at $\theta = 90^0$). The support shell and cryostat

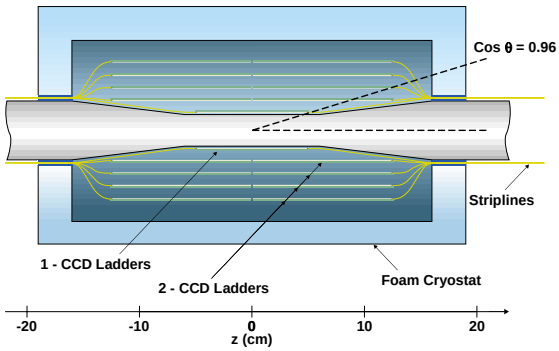


**Figure 1.** Detector cross-section. Five layers provide robust standalone tracking capability, with 3-hit coverage to $|\cos\theta| = 0.96$.

(upper two contributions to the plot) barely affect the impact parameter resolution. Ideas for achieving this detector thickness are discussed in Section 3.

As with SLD, it is not necessary to read out or time-stamp the data at the level of single bunch crossings. What is needed is to have sufficiently short readout time to keep the layer-1 occupancy to an acceptable level. This is discussed in Section 4. Simulations of the detector performance lead to an estimated impact parameter resolution of $3.8\ \mu\text{m} \oplus 6.6\ \mu\text{m}/\,p\sin^{3/2}\theta$ for both the $r\phi$ and $rz$ projections [4]. $p$ is the track momentum in GeV/c. This single track performance ensures pure, efficient *b* and *c* jet tagging, as well as efficient measurement of vertex charge, charge dipole and other important characteristics of heavy flavour jets. The main open question is whether the construction of such an adventurous detector will be possible. In the remainder of this paper we discuss the R&D programme under way to bridge the gap between the SLD detector and what will be required for the future LC.

## 3. LAYER THICKNESS

Given that CCD vertex detectors are operated at cryogenic temperatures (typically 180 K) to suppress loss of charge transfer efficiency from radiation damage, it has always been necessary to adopt a mechanical design that minimises stresses due to differential contraction. In SLD this was achieved by a rigid beryllium support shell, in which the detector elements (ladders) were supported with fixed joints at one end, sliding at the other, by means of an 'annulus block' fixed to the support shell and a 'ladder block' fixed to the ladder. These blocks were held in contact by a compression spring, with one degree of freedom established by vee-and-flat contact areas between the blocks.

The same principle is suggested for the future LC detector, with two differences. The relatively rigid ladder of SLD becomes a bare silicon CCD, thinned to ~ 50 $\mu$m by an industry-standard back-thinning procedure. The structure is stabilised by a tensioning spring, as shown in Figure 3. The outer ladders of the detector (beyond layer 1) are of length 25 cm; these will consist of two CCDs placed end-to-end, and joined with a thin silicon bridging strip. Initial studies with mechanical models constructed with thin silicon show excellent stability. For a modest spring tension

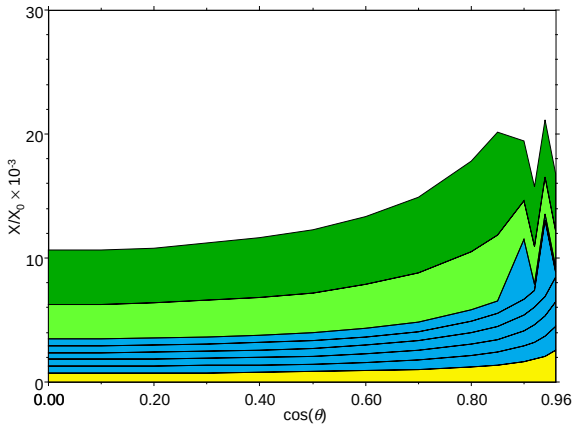


**FIGURE 2.** Material budget.

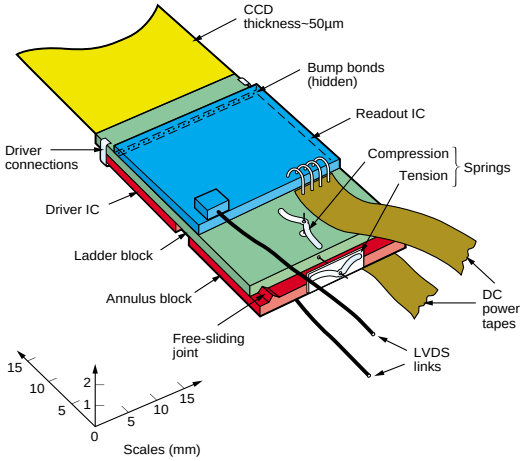


**FIGURE 3.** Ladder end. The silicon CCD is bonded to the ladder block which also carries the inner electronics; the CCD is tensioned by the spring acting between the ceramic blocks.

above 150 gms, the stability in the sagitta of the ladder when the spring force was repeatedly released (allowing the ladder to sag by several mm) and reimposed was less than 3 $\mu$m. These tests need to be extended in various ways to completely establish that the concept will work, but it looks extremely promising.

## 4. READOUT ARCHITECTURE

As already mentioned, it is necessary to read out the detector sufficiently rapidly to keep the background hit occupancy below about the 1% level. For the inner layer, this implies readout over about 100 bunch crossings at either NLC or TESLA. In the former case (190 bunches per train) one can integrate through the train and read out in the 8 ms between trains. This requires a modest development from the SLD readout system, with a factor 5 higher readout rate and some subdivision of the readout register.

In the case of TESLA (3000 bunches per train at 500 GeV) the situation is more challenging. It is necessary to read the detector ~ 20 times *during* the train. This requires a novel CCD architecture (column-parallel) in which the readout register is eliminated and the signals from each column are deposited in parallel on the gates of a series of transistors, whose output signals are connected by bump-bonding to an adjacent readout chip outside the active volume of the detector. This readout chip, fabricated in submicron CMOS, has precedents in the peripheral processing logic currently being developed for CMOS imaging systems. The design philosophy of this hybrid approach is to combine the capability of CCD manufacturers for wafer-scale devices using image stitching technology for device manufacture, with the capability of submicron CMOS for packing the required logic into the 20 $\mu$m column width. The readout chip will include signal amplification, analogue-digital conversion, pixel thresholding, cluster signal thresholding based on a $2\times2$ kernel (combining information from adjacent columns), and memory. The sparsified data from the 20 or so readout sequences during the bunch train would be stored in these local memories (about 10 Mb for the entire vertex detector), and downloaded into the off-detector

processor selected to handle the full TESLA detector data for that bunch train, via a few optical fibres at each end of the detector. This processing could take several seconds, so there would be about one hundred of these processors, with data from the next train downloaded to a different available processor in the farm.

In order to control backgrounds, the inner layer CCDs of the TESLA detector should be clocked at a frequency of ~ 50 MHz, which will require special CCD processing. Preliminary discussions with manufacturers suggest that these developments are well within the limits of technology. SPICE simulations of a CCD having realistic parameters indicates no problem with 50 MHz clocking; relevant test structures will be included in the LCFI R&D programme.

The CCD clock drive pulses should be generated locally on a driver IC having a low inductance connection to the CCD as sketched in Figure 3. The CCD is bonded to the ceramic ladder block, and is overlaid by the readout IC with the row of inter-connecting bump bonds. The driver IC is attached to the underside of the same block. Simulations indicate that the power dissipation in the entire detector volume will be only 9 W. As at SLD, this volume can be cooled by a gentle flow of nitrogen gas, with no impact on the material budget. The ICs on the ends of the ladders will require a more robust cooling system. The evaporative cooling with liquid nitrogen as used on the NA11 experiment at CERN [5] provides a likely solution.

## 5. CONCLUSIONS

We have about 5 years of R&D before the technology choice for the future LC needs to be made. This choice could be influenced by which accelerator design is selected. CCDs while promising, could run up against show stoppers such as a lack of sufficient R&D investment, or an unexpectedly hostile radiation environment (specially neutrons). Therefore, for all the pixel options, it is important to push the development vigourously. The challenge of achieving the performance needed to do the physics is considerable, but the physics output could be immense.

In any case, this is not a 'winner takes all' situation. The various silicon pixel technologies are in demand for many applications, each with its own current and future preferred niche applications. For the future LC, the optimal vertex detector design will surely evolve during the life of the machine. Therefore, it is essential to ensure convenient access to the inner detector region in order to permit upgrades (vertex detector, beam-size and position monitors, etc) as the technology advances. In this respect, the future LC is likely to have similar access requirements to earlier colliding beam machines (LEP, SLC, etc). In the case of the TESLA detector, a convenient access procedure similar to that adopted at SLD is included in the design.

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