CCD-based vertex detector for the linear collider

Status report from the Linear Collider Flavour ID Collaboration (LCFI)

Chris Damerell
29 March 2000

- Overview
- Low-mass detector
- Fast readout
- Radiation resistance
- Performance criteria
- Technology choice for LC vertex detectors

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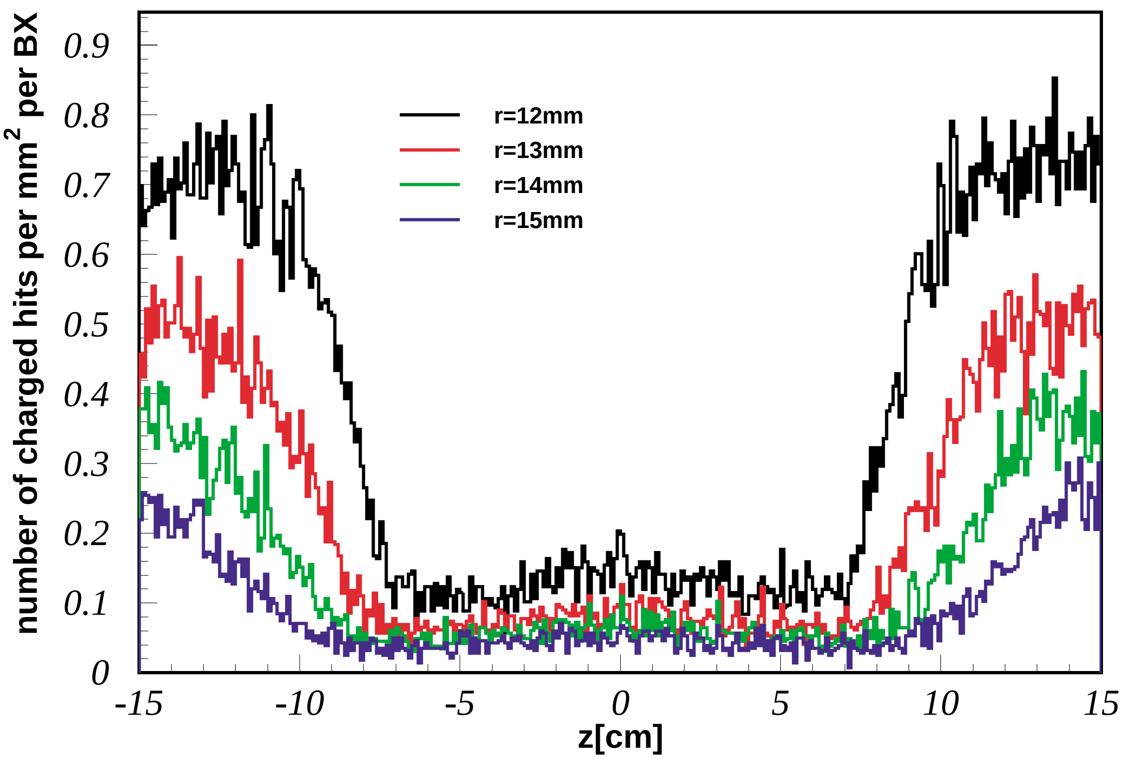
Overview

- Design concept stable since Snowmass '96
  - concentric cylinders
  - maximum polar angle coverage
  - 5 layers
  - standalone tracking

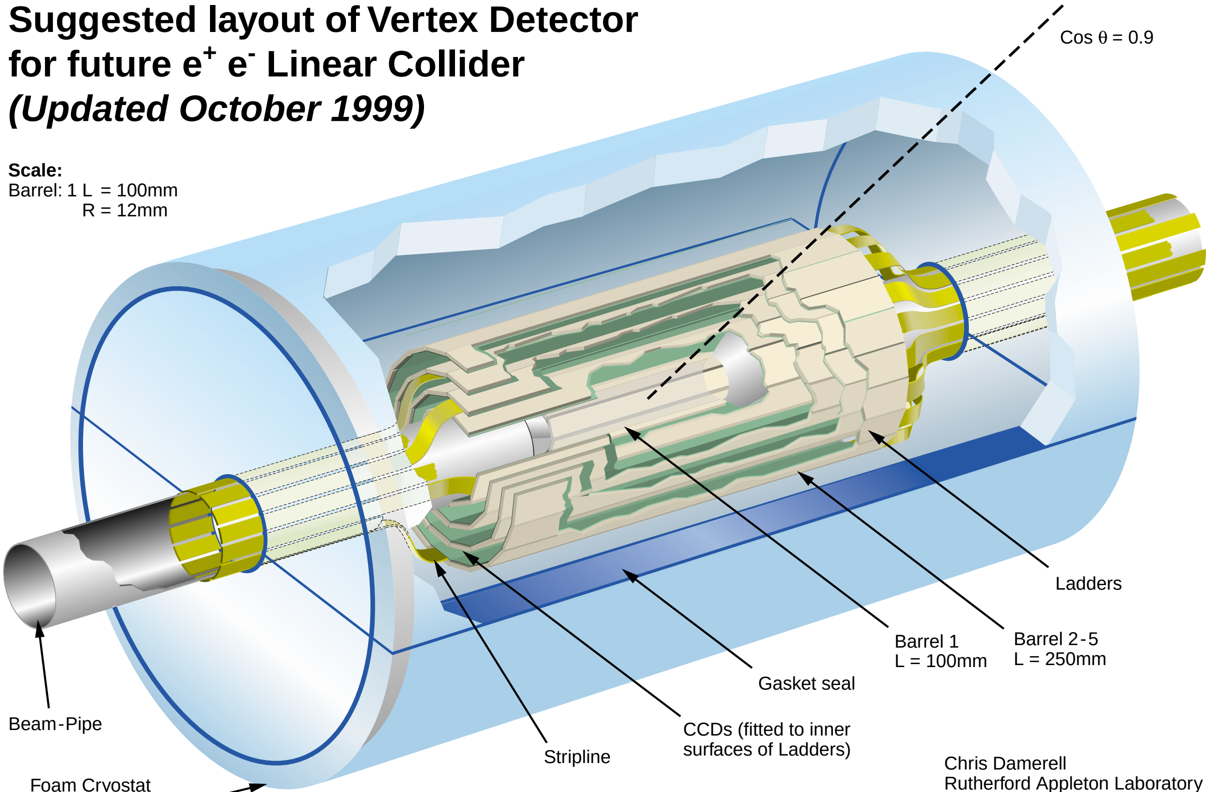
- Recent studies in context of TESLA interaction region
  - 4 Tesla solenoid
  - R_{bp} = 14 mm
  - L1 active length = 100 mm
  - 3-hit coverage including L1 to

    $\cos\theta = 0.955$


number of charged hits per mm^2 per BX
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-15
-10
-5
0
5
10
15
z[cm]
r=12mm
r=13mm
r=14mm
r=15mm

Suggested layout of Vertex Detector for future $e^+ e^-$ Linear Collider *(Updated October 1999)*

Scale:
Barrel: 1 L = 100mm
R = 12mm



Chris Damerell
Rutherford Appleton Laboratory
October 1999

- Layer thickness
  - official goal 0.12% X_0
  - may reduce to ≤ 0.06% X_0
  - ideas for a similarly thin inner beam-pipe
- Fast readout
  - conventional clocking at 50 MHz will suffice for NLC
  - TESLA bunch structure is more challenging
    → column-parallel CCD
  - this development resonates with requirements in several other areas of science
- Radiation resistance
  - Tooling up for R&D
- Technology choice
  - Physics goals:
    - high efficiency/purity for charm jet ID
    - measurement of vertex charge (for separating b from $\bar{b}$ and c from $\bar{c}$)
    - measurement of charge dipole (for separating b from $\bar{b}$ in jets with neutral Bs)

- use of p_T imbalance to correct vertex mass for missing neutrals including neutrinos

- The most optimistic current thinking will fall short of these goals, so we need to push for best possible performance in all critical parameters:
    - R_{bp}
    - layer thickness
    - (point measurement precision)

- Technology choice will be determined by who manages to meet their design goals, including:
    - thermal management (10s or 100s of watts)
    - full material budget (supports, cables etc)
    - overall mechanical stability
    - *sufficient* robustness wrt charged particle and neutron backgrounds

- Very open between:
    - CCDs
    - monolithic APS
    - hybrid APS

    Only clear decision is for a silicon pixel-based system as pioneered at SLD

Low-mass detector

- Our official goal is 0.12% X_0 per layer

  (30 μm silicon bonded to 250 μm beryllium substrate in form of omega or vee beam)

- Unsupported-silicon option (under tension) could reduce this by a factor two, to 0.06% X_0, assuming 60 μm die thickness

- Assisted by the strong technology evolving for paper-thin packages (PTP)

- R&D programme consists of

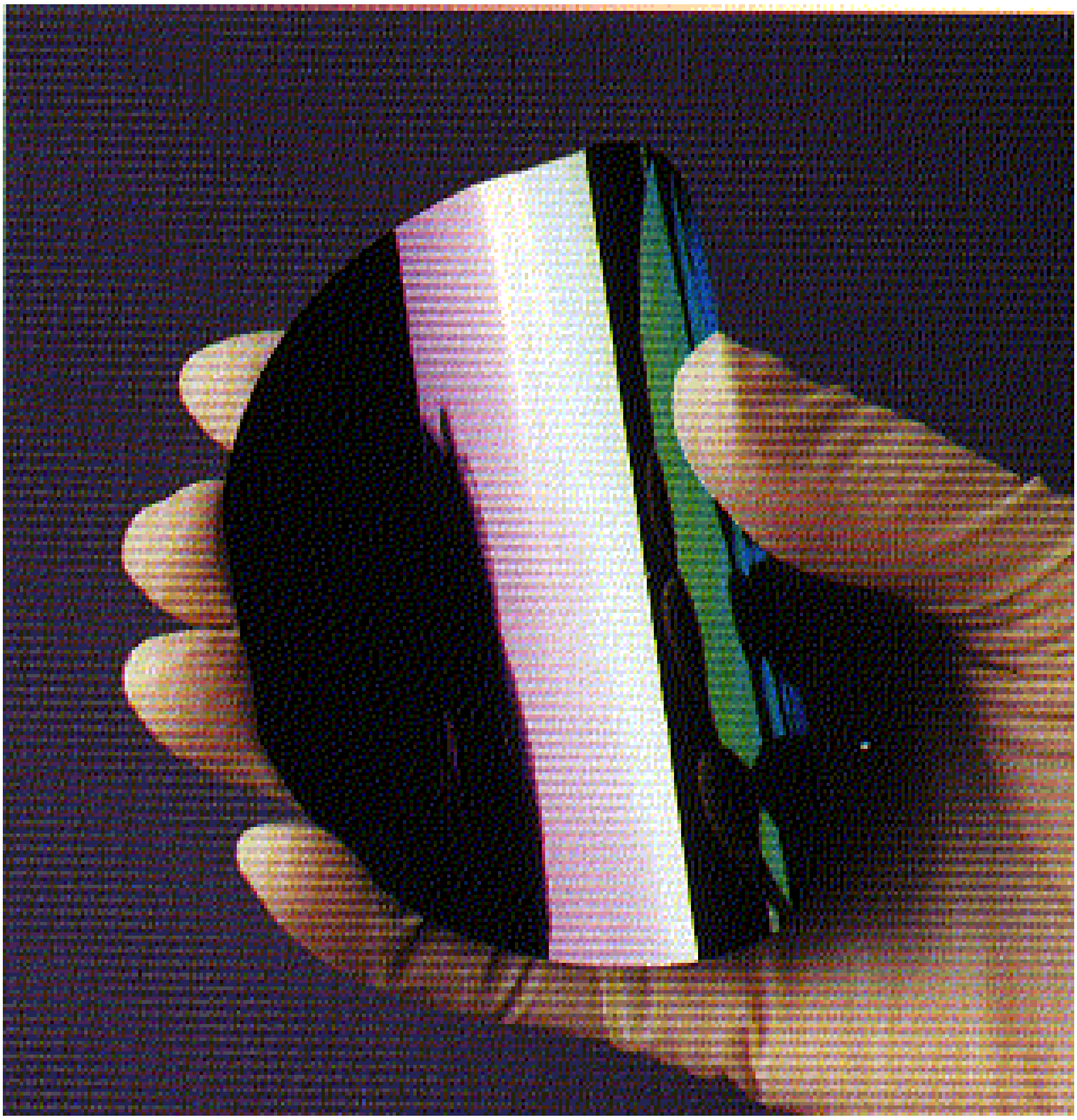
  - tests with unprocessed silicon

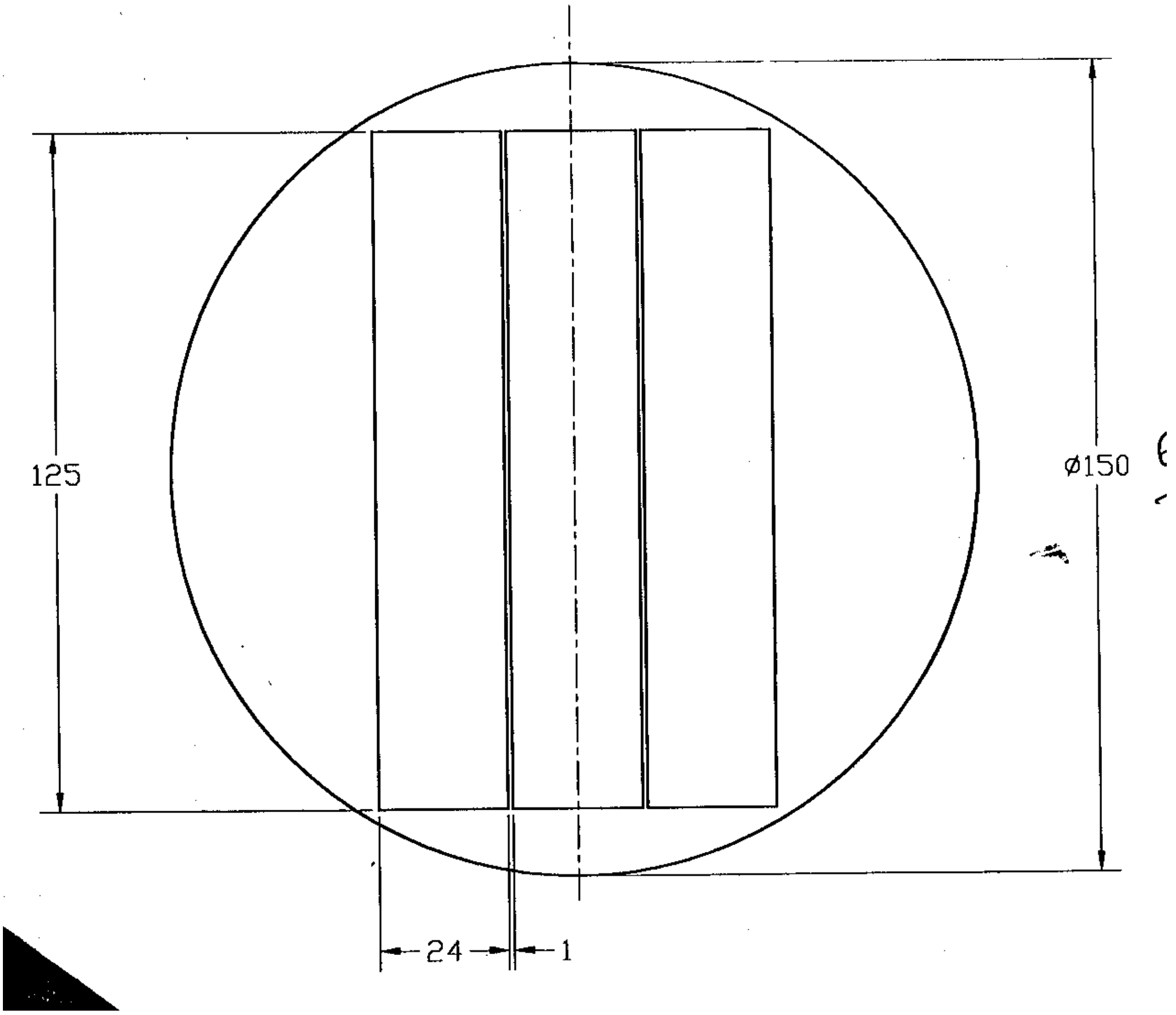
  - tests with thinned CCDs

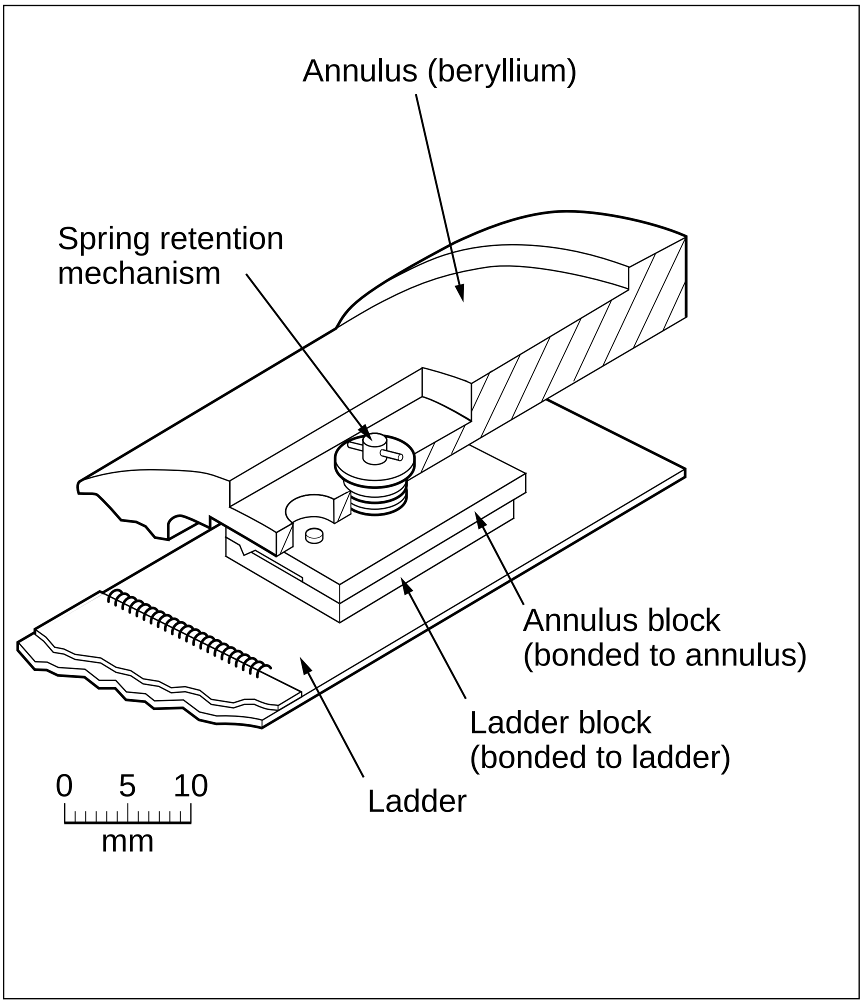
- Supports will consist of annulus block/ladder block assemblies as used in SLD, with an additional tensioning spring

- If successful, this approach will put pressure to reduce beam-pipe thickness to 0.25 mm (0.07% X_0) or lower. This may be feasible if VXD support shell is used for strain relief, particularly important during installation/removal of inner detector assembly

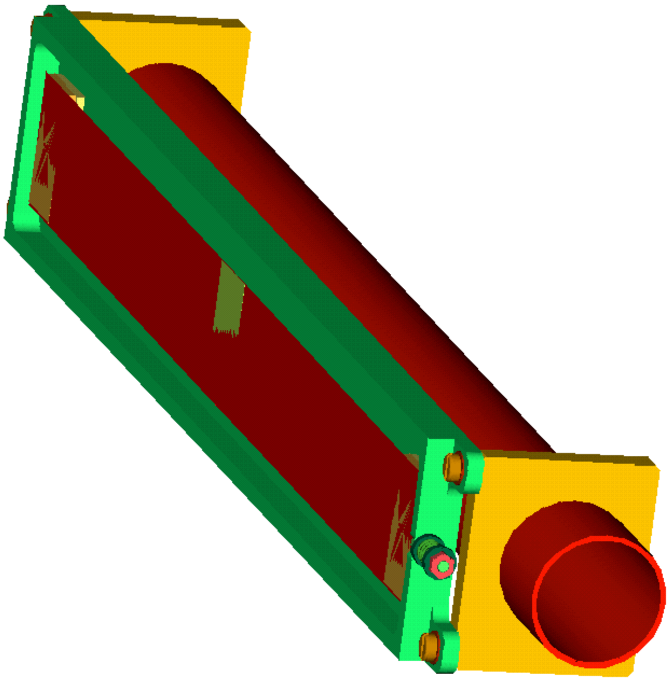
Virginia Semiconductor



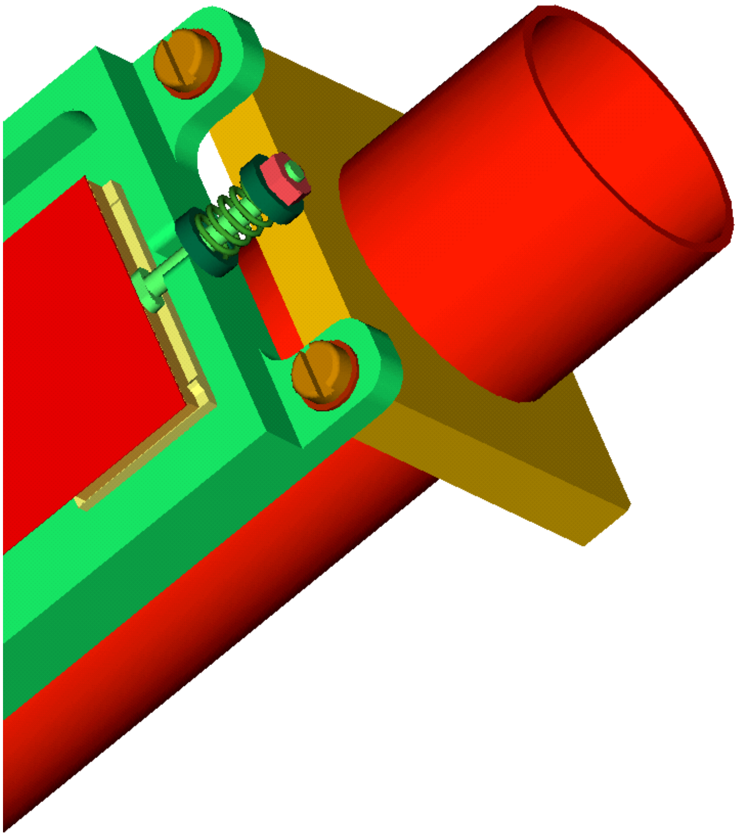

125
ø150
24
1

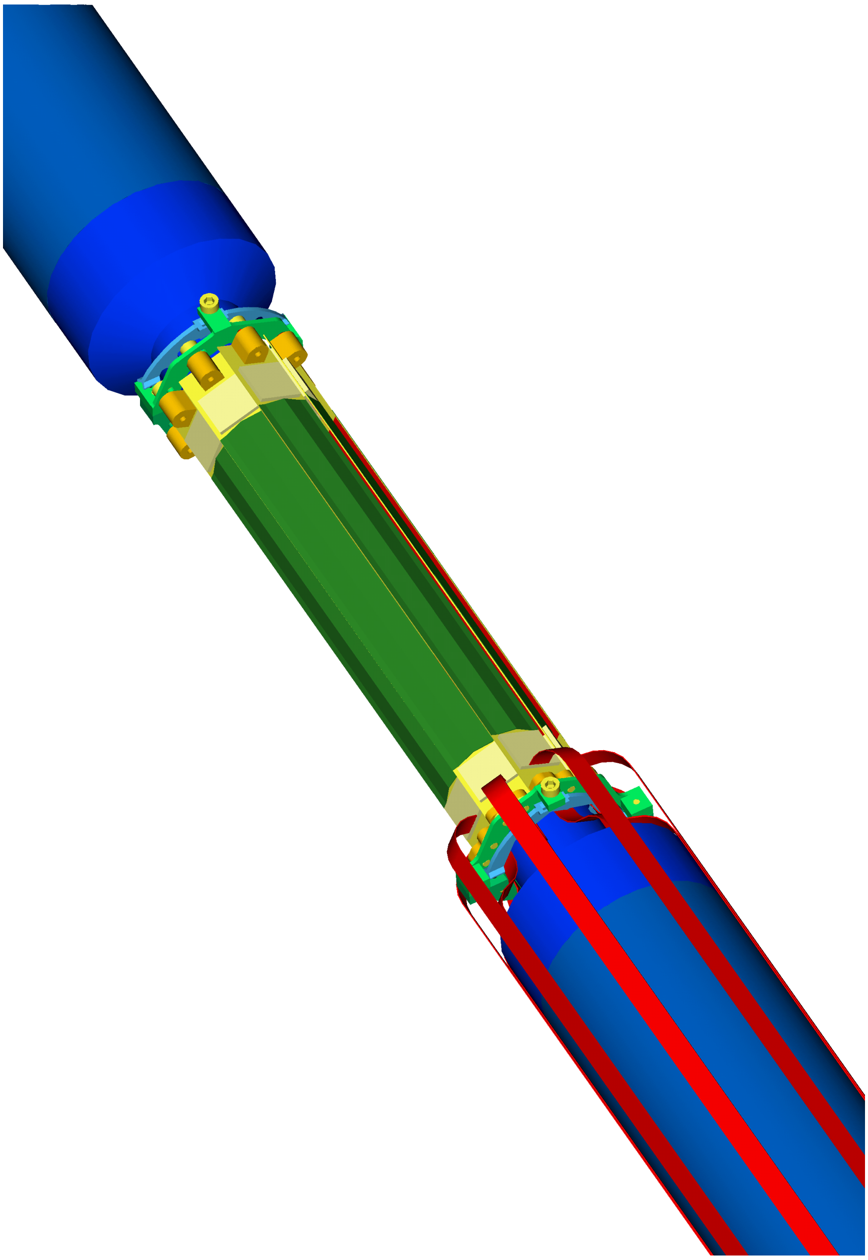

Annulus (beryllium)
Spring retention
mechanism
Annulus block
(bonded to annulus)
Ladder block
(bonded to ladder)
Ladder
0 5 10
mm

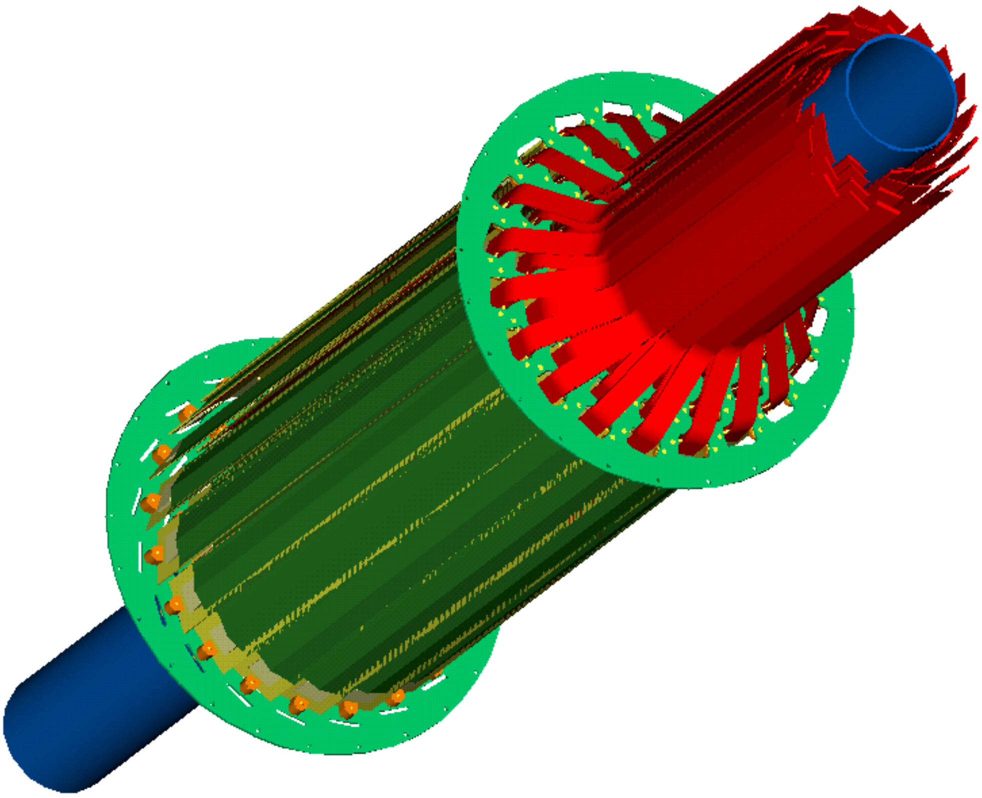
Unsupported silicon ladder



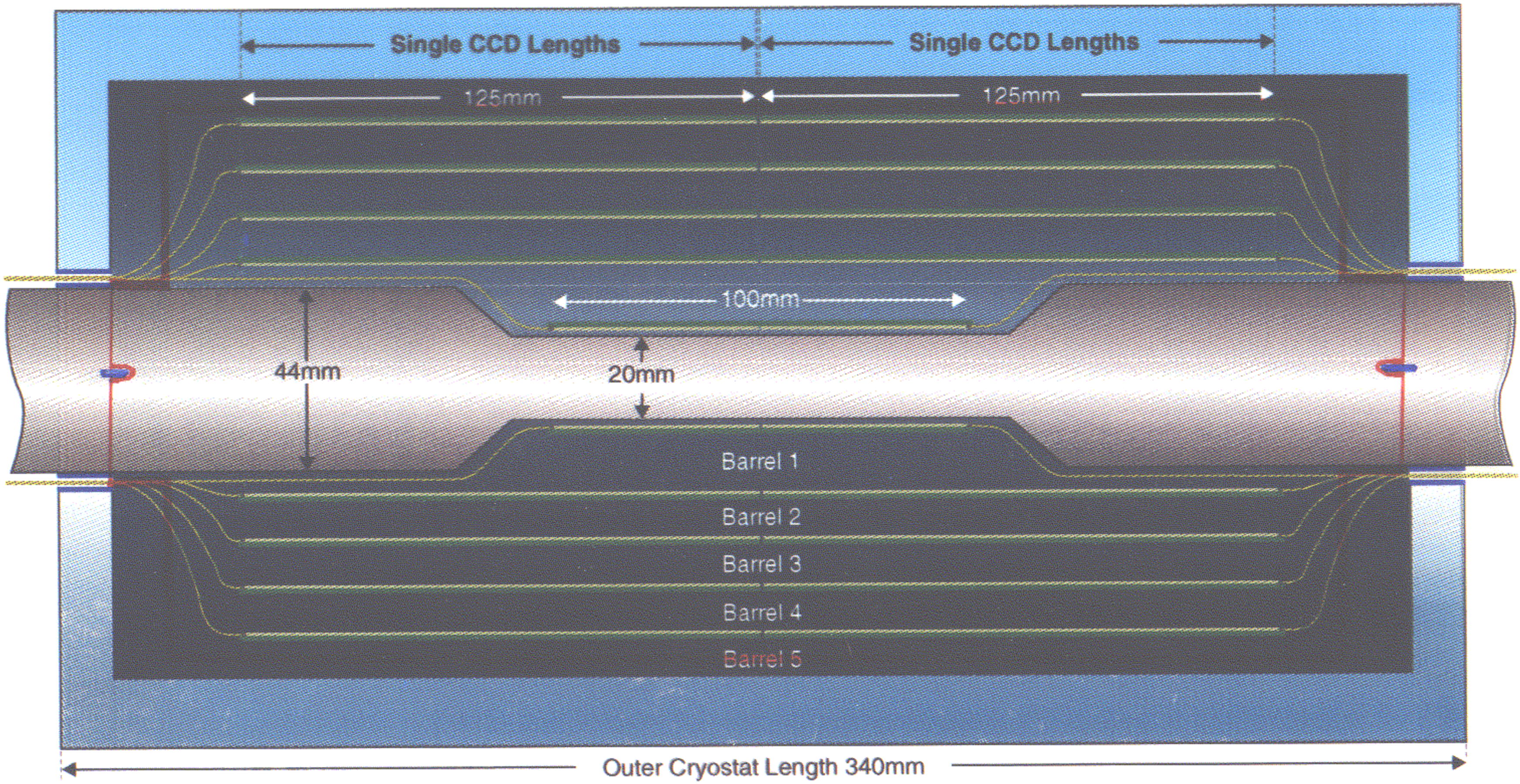
Details of tensioning system







Suggested layout of Vertex Detector for future $e^+ e^-$ Linear Collider (*Updated October 1999*)



Fast Readout

- Column-parallel readout with a single row of staggered bump bonds on 60 μm pitch follows standard industrial practices (unlike large area bump bonding)

- Minimising electronics suggests a no-reset output with resistive load

- Feasible clocking rate depends on many parameters:

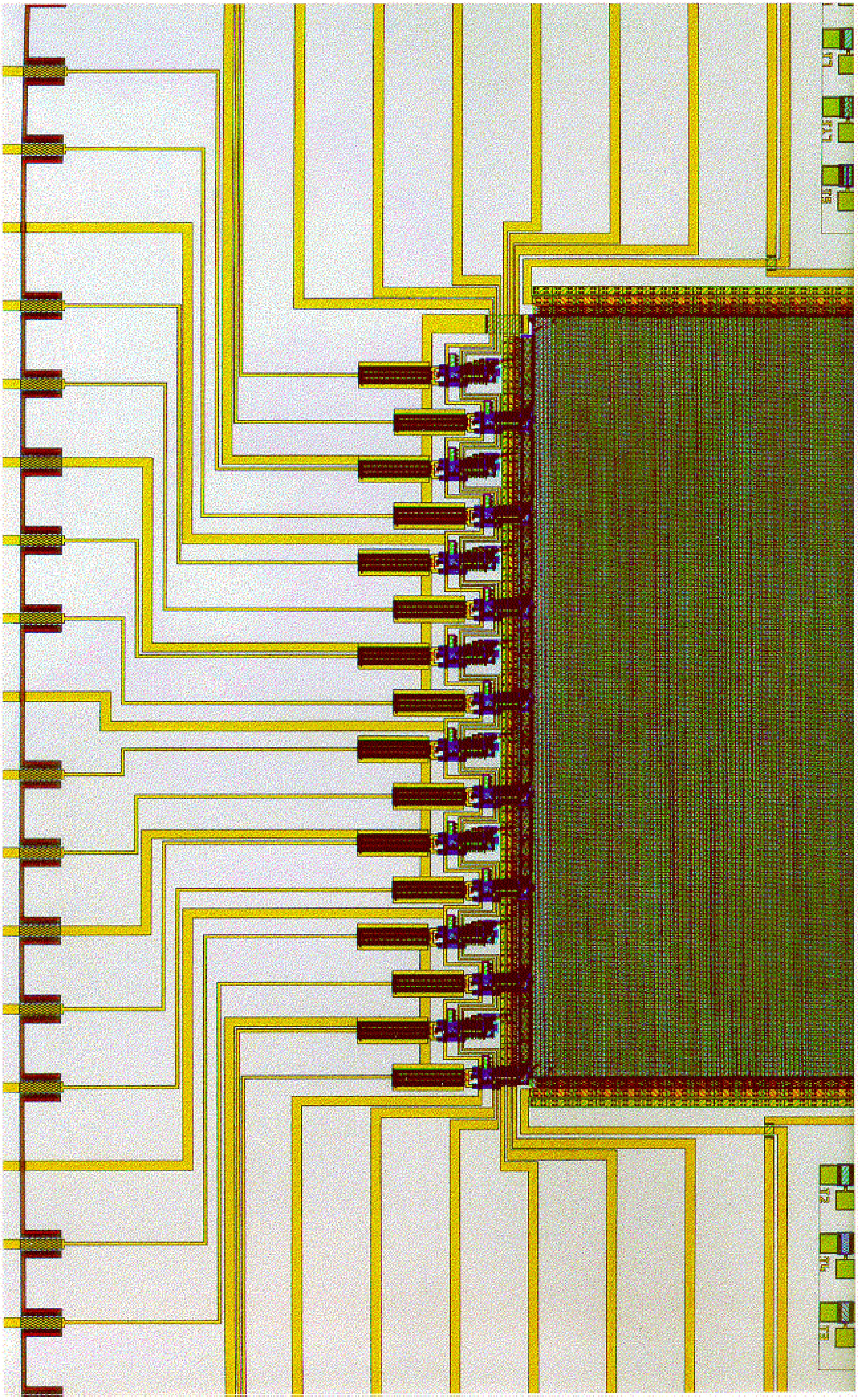
  - clock voltages (1-3 V)

  - I gate capacitance (function of CCD operating conditions)

  - cooling power at ends of ladders beyond vertexing aperture

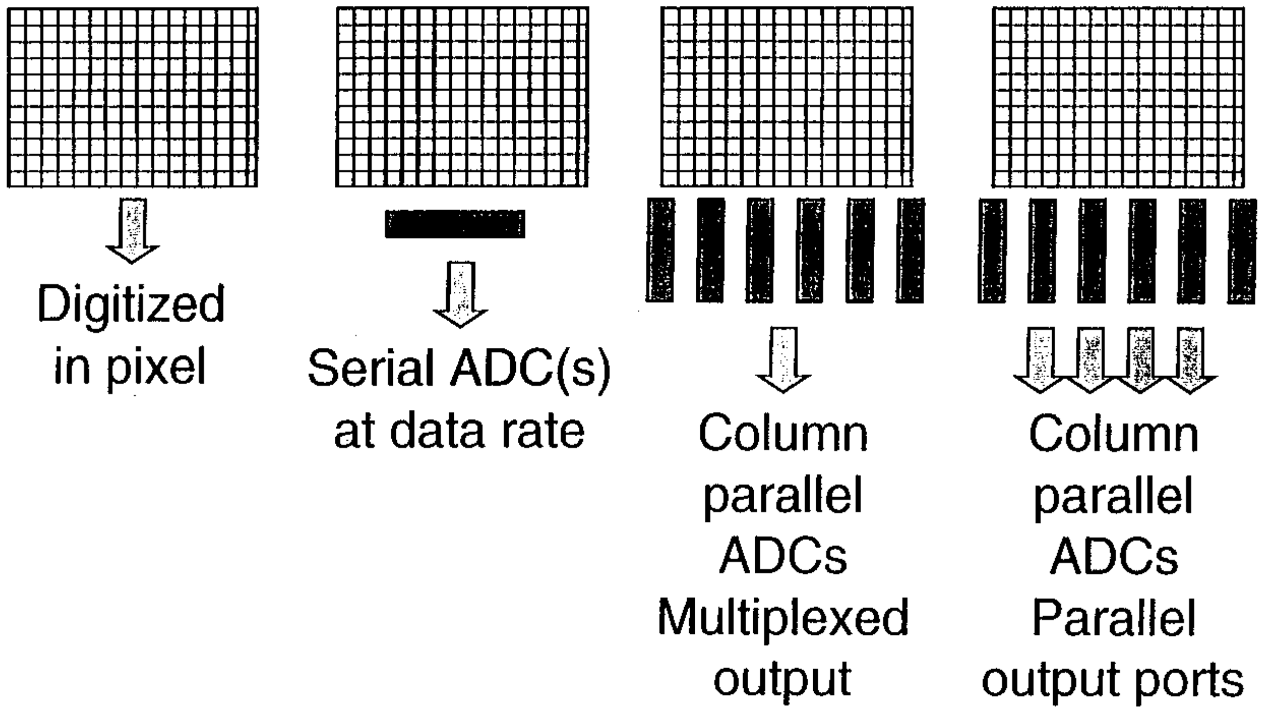
  - developments in driver IC design

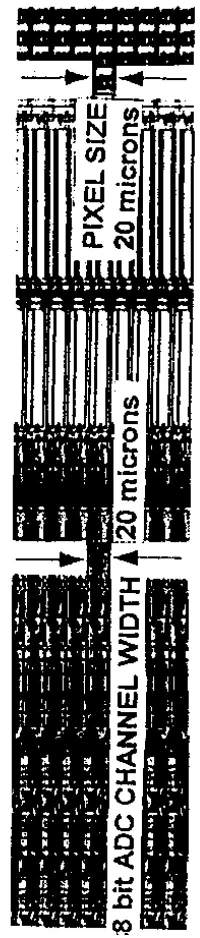
- Signal processing looks like a project well matched to 0.25 μm CMOS technology. Power dissipation?

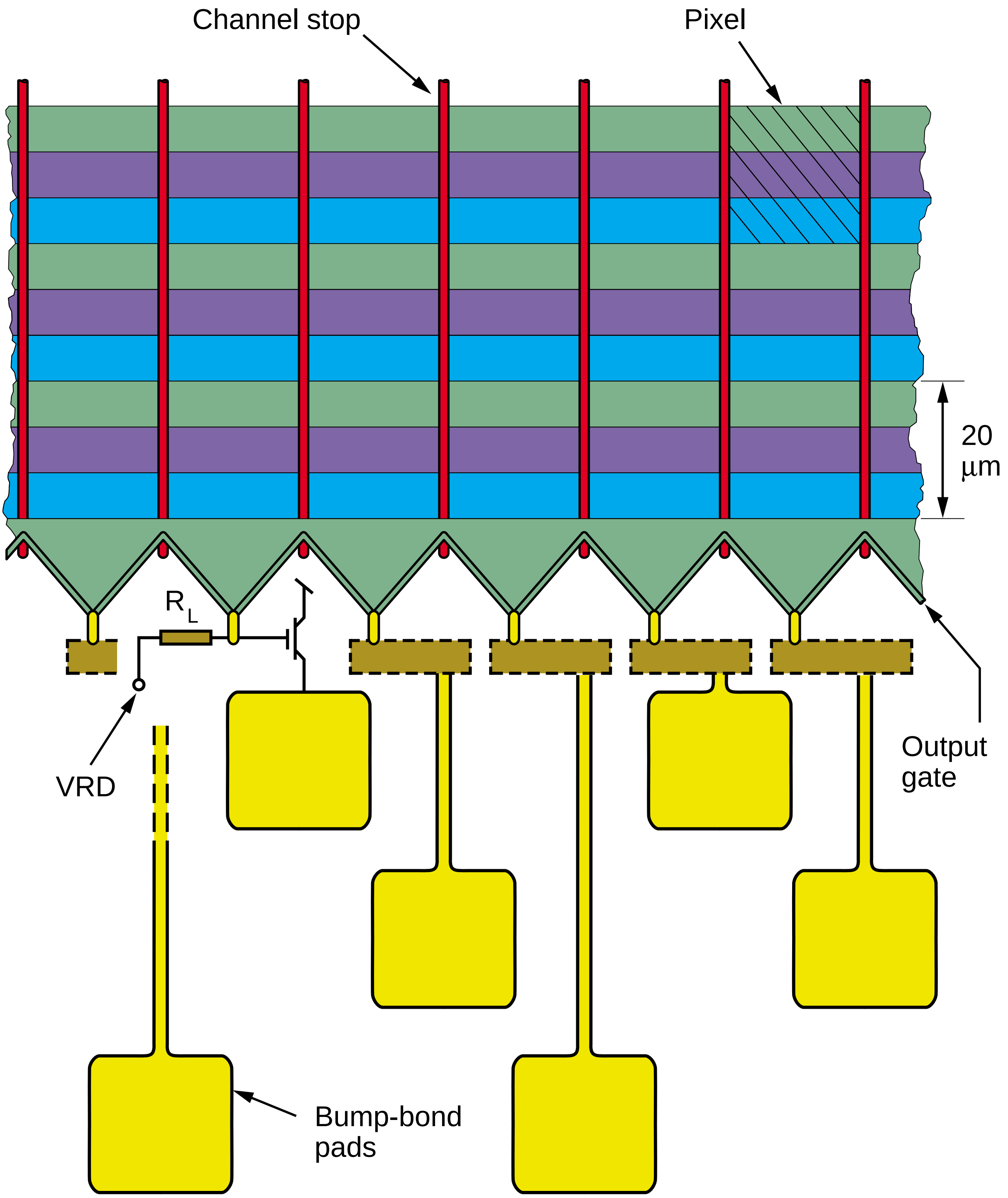


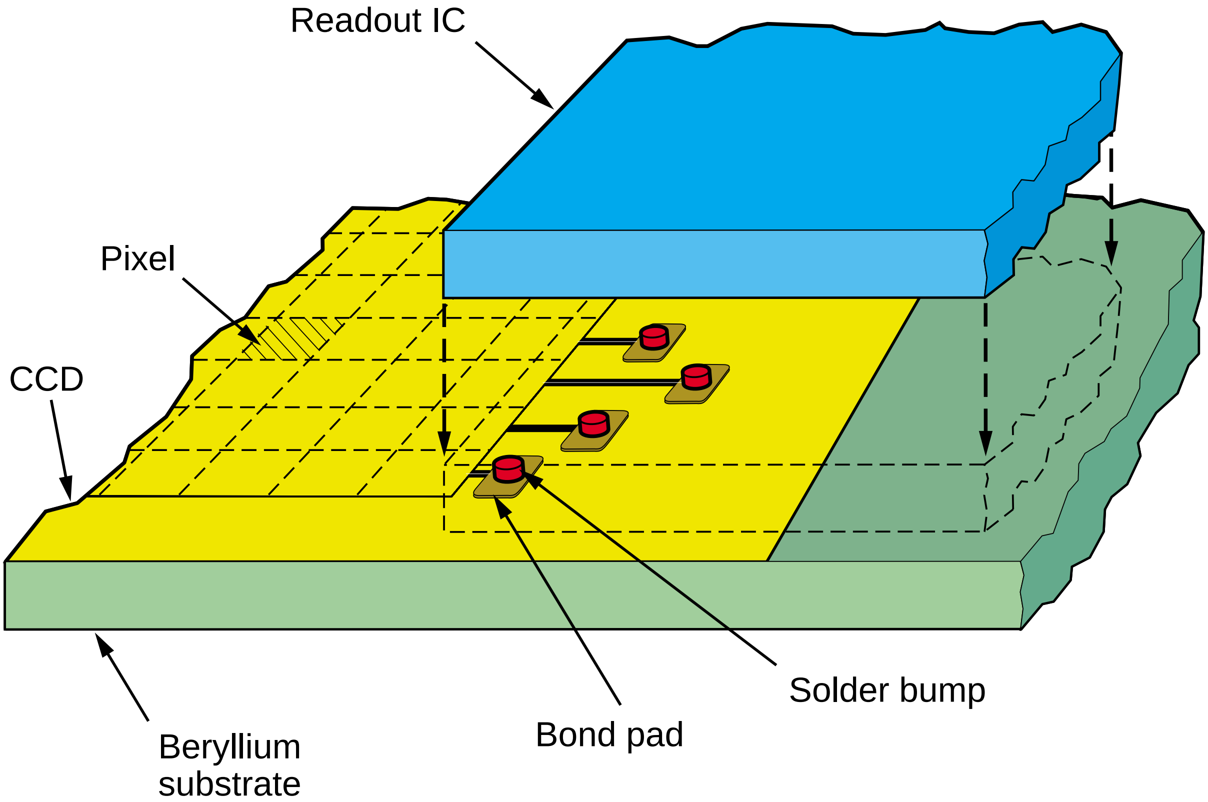
ON-CHIP ADC ARCHITECTURES

Photobit

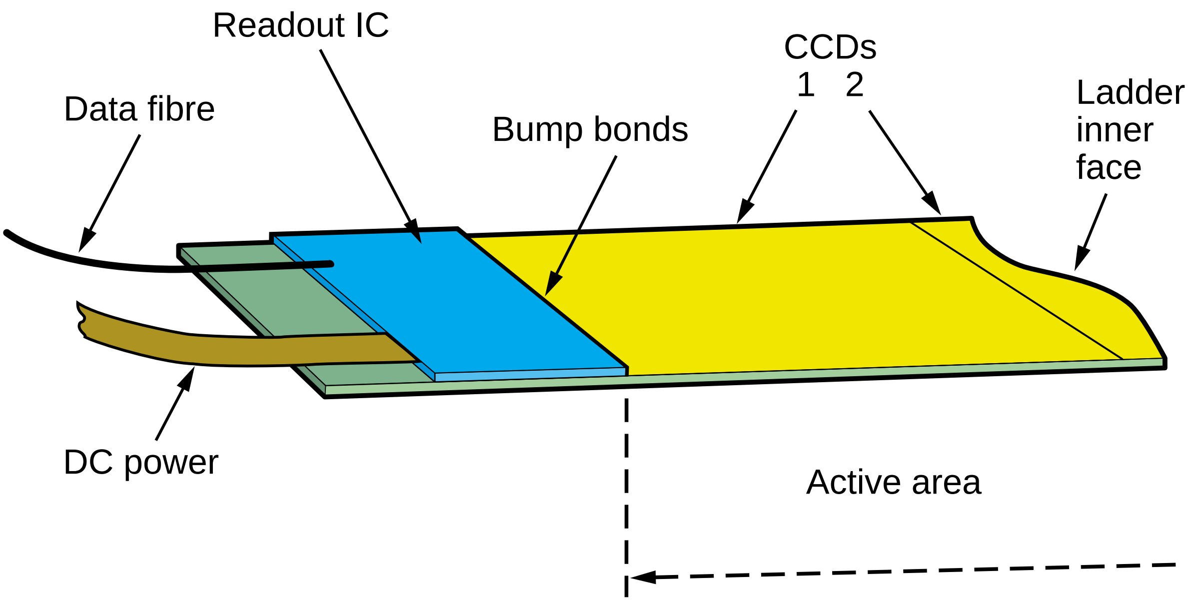





Channel stop
Pixel
20 μm
R L
VRD
Output gate
Bump-bond pads


Readout IC
Pixel
CCD
Solder bump
Bond pad
Beryllium substrate

Layout of ladder end



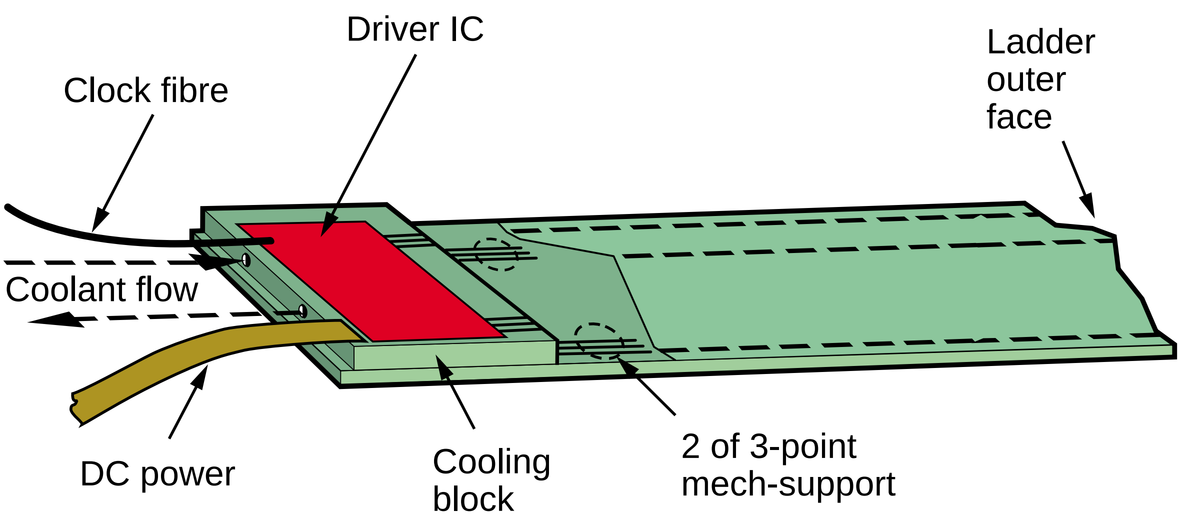
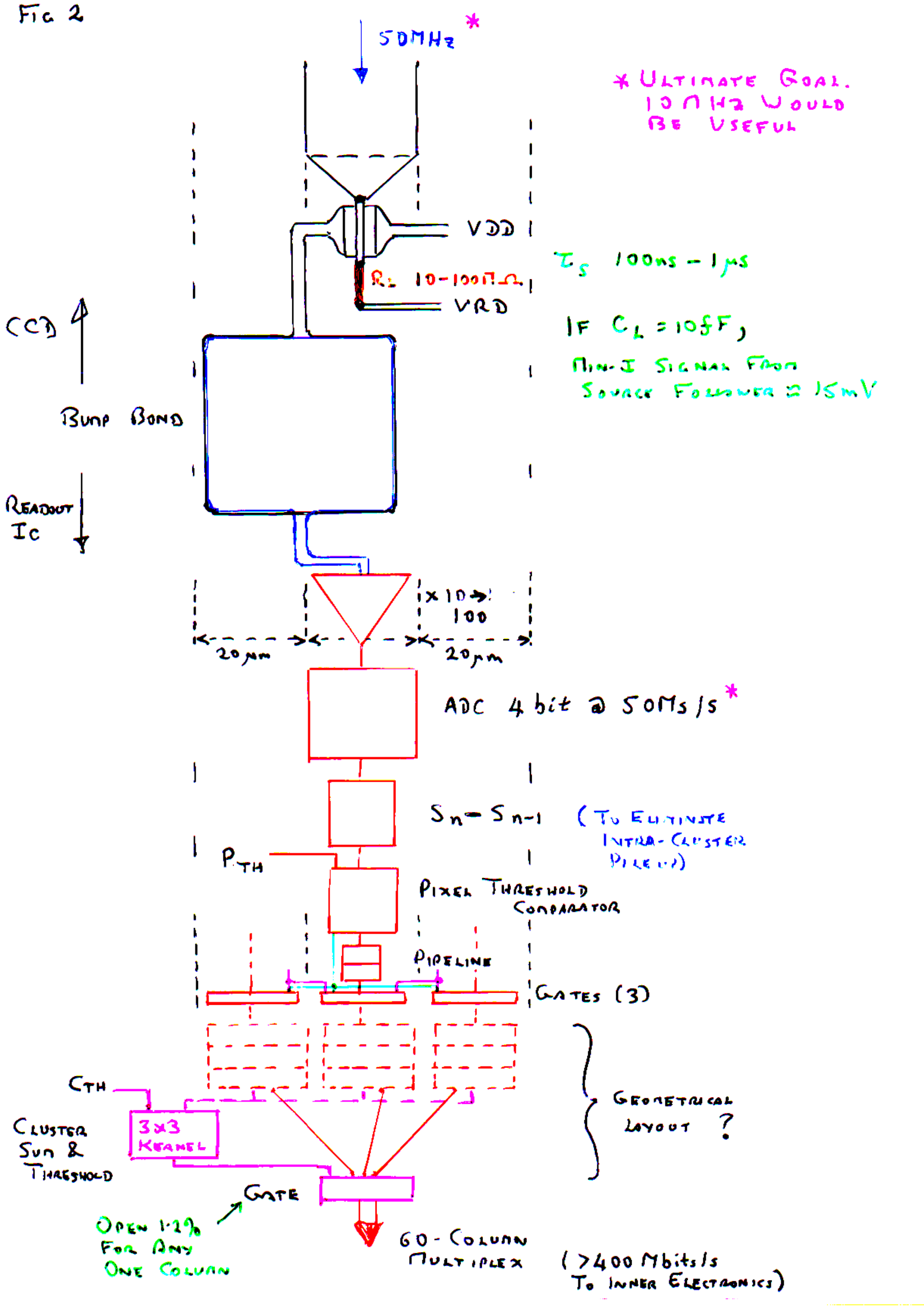
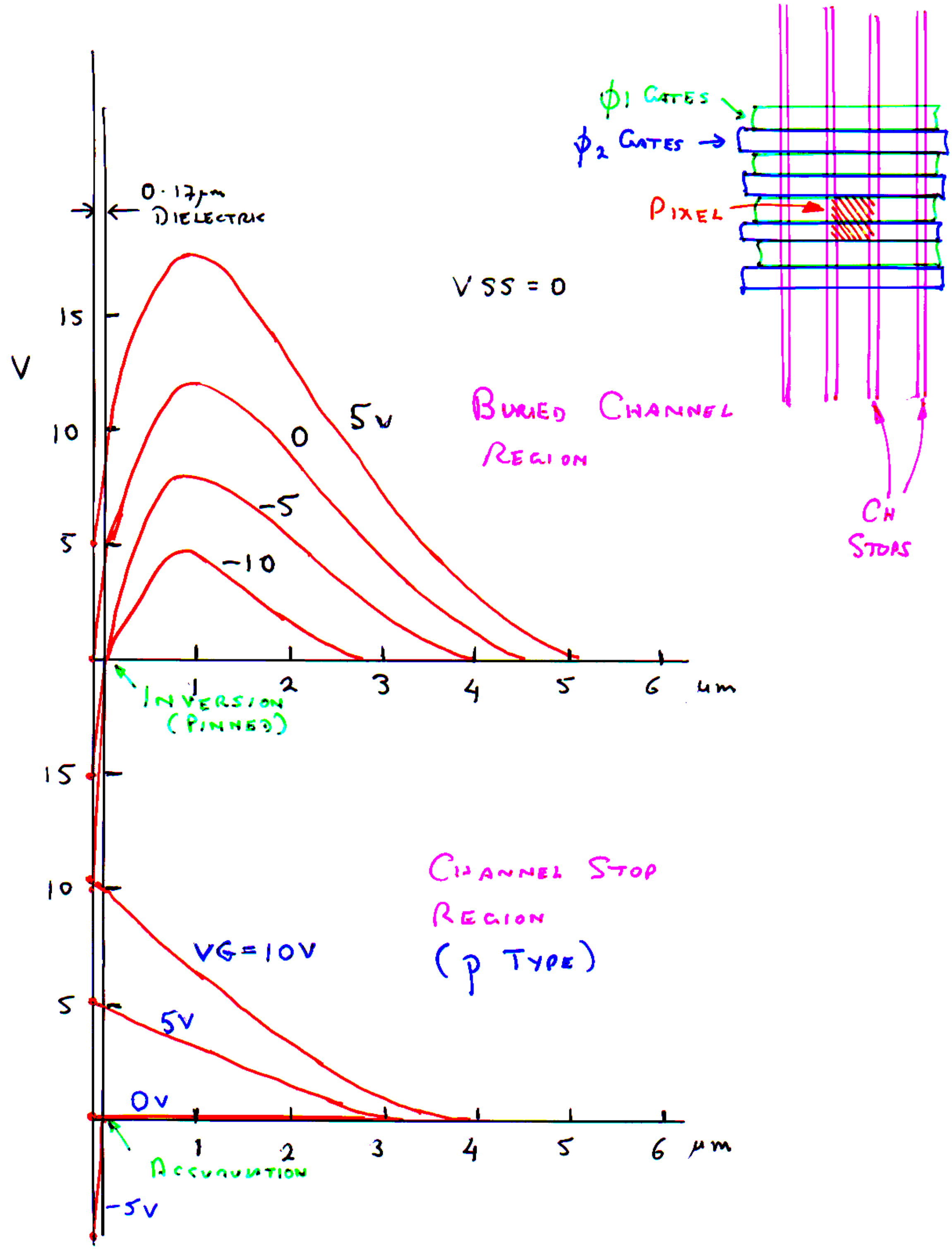
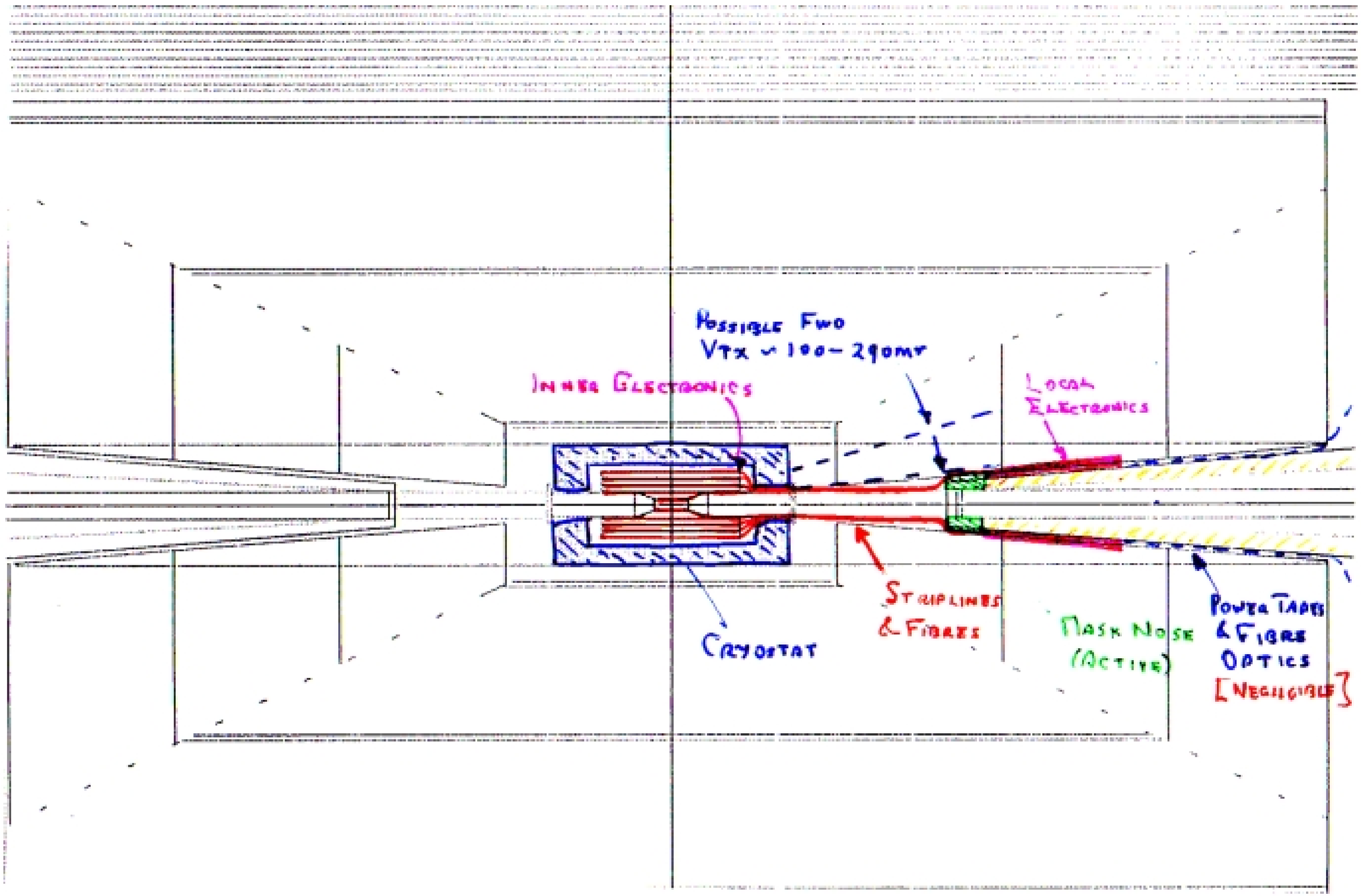


FIG 2


50MHz *
* ULTIMATE GOAL. 10MHz WOULD BE USEFUL
VDD
RL 10-100kΩ
VRD
τS 100ns – 1μs
IF CL = 10fF,
MIN-I SIGNAL FROM SOURCE FOLLOWER ≃ 15mV
CCD
BUMP BOND
READOUT IC
x10 → 100
20μm
20μm
ADC 4 bit @ 50Ms/s *
Sn – Sn-1
(TO ELIMINATE INTRA-CLUSTER PILE-UP)
PTH
PIXEL THRESHOLD COMPARATOR
PIPELINE
GATES (3)
GEOMETRICAL LAYOUT ?
CTH
CLUSTER SUM & THRESHOLD
3x3 KERNEL
GATE
OPEN 1-2% FOR ANY ONE COLUMN
60-COLUMN MULTIPLEX
(>400 Mbits/s TO INNER ELECTRONICS)



0·17μm
DIELECTRIC
VSS = 0
V
15
10
5
5V
0
-5
-10
BURIED CHANNEL REGION
1
2
3
4
5
6
μm
INVERSION (PINNED)
φ1 GATES
φ2 GATES
PIXEL
CH STOPS
15
10
5
VG=10V
5V
0V
-5V
CHANNEL STOP REGION
(p TYPE)
1
2
3
4
5
6
μm
ACCUMULATION

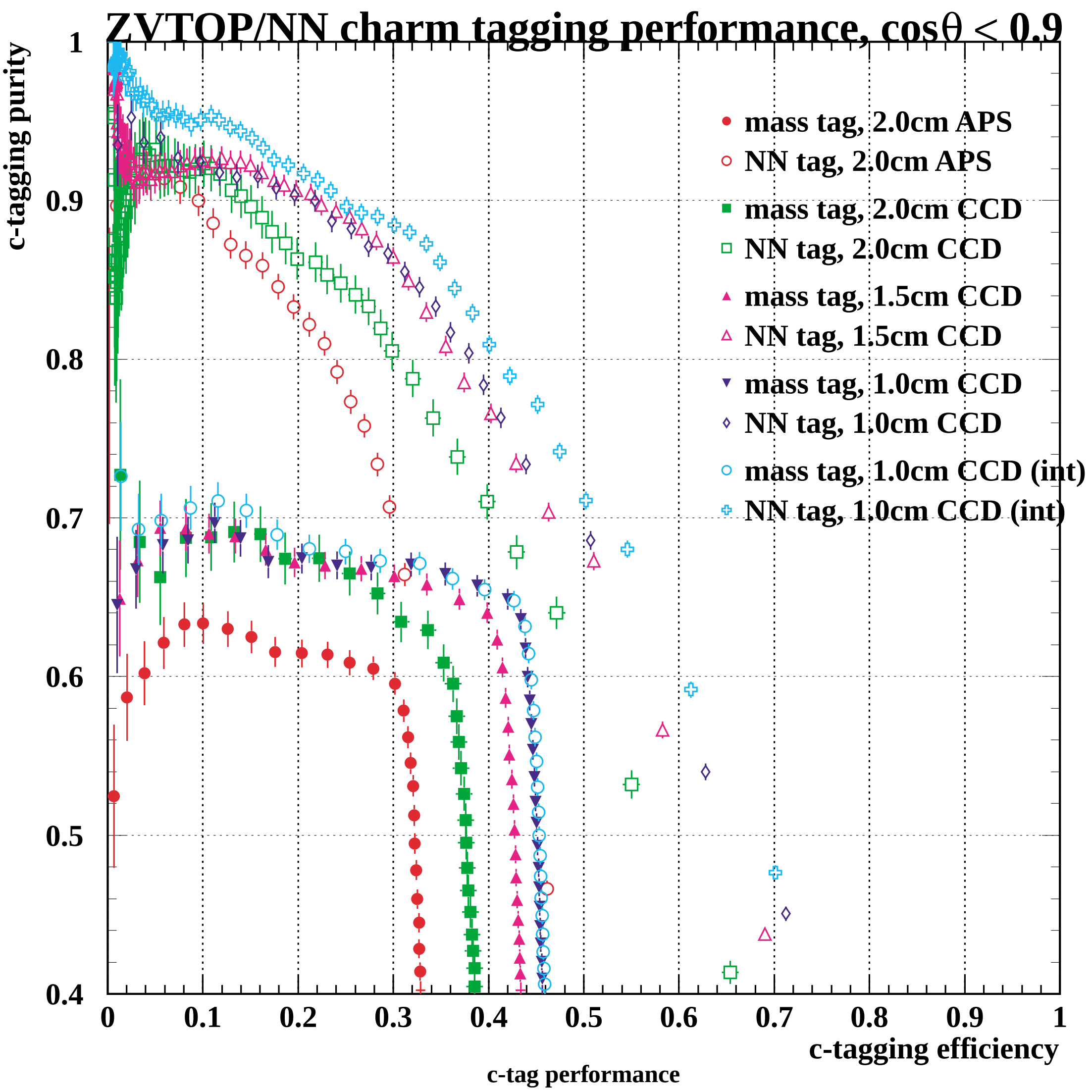


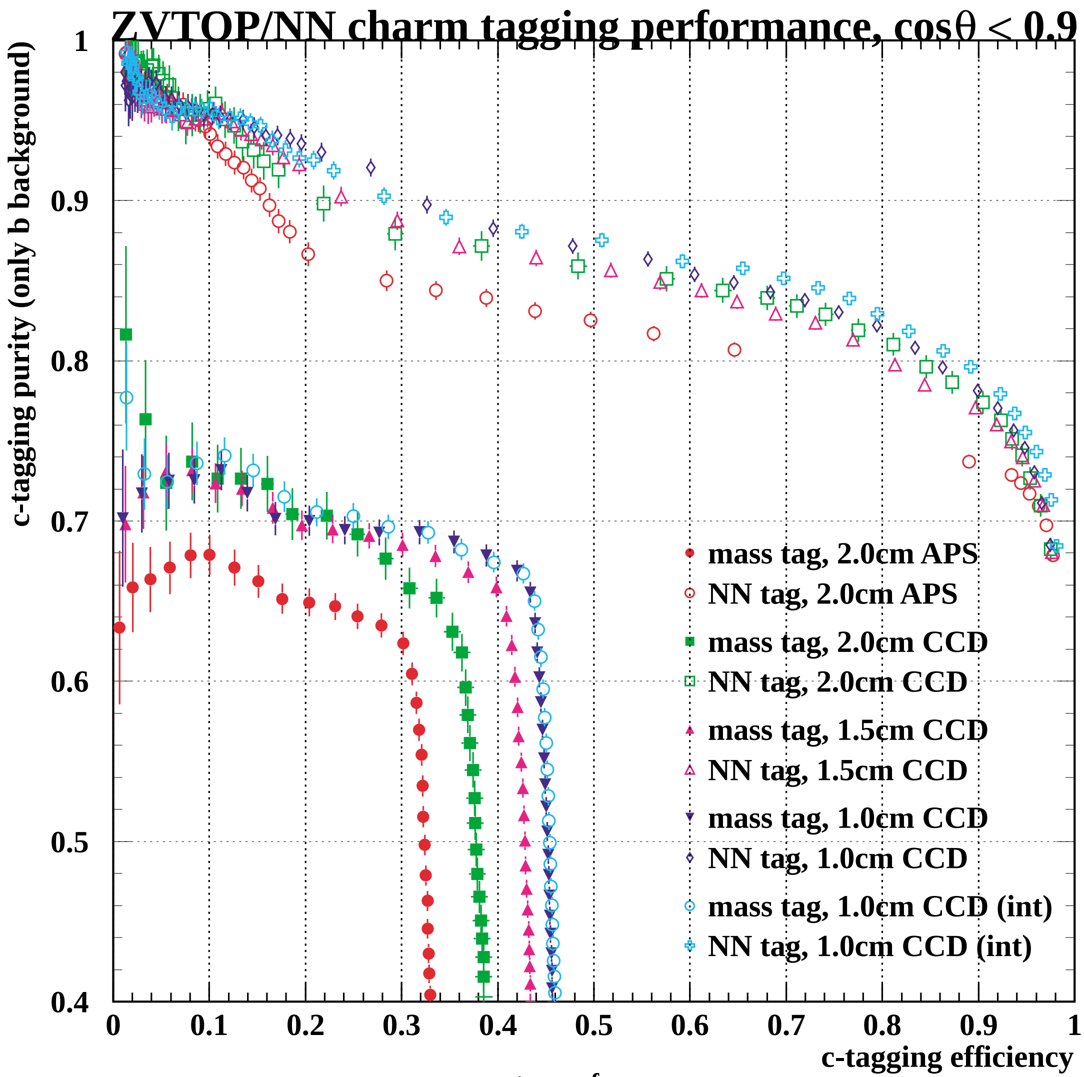
Possible Fwd
Vtx ~ 100 - 290mr
Inner Electronics
Local
Electronics
Cryostat
Striplines
& Fibres
Mask Nose
(Active)
Power Tapes
& Fibre
Optics
[Negligible]

Performance criteria

- Current state-of-art tagging from Richard Hawkings; development of Dave Jackson's ZVTOP
- Ghost-track extensions in SLD suggest room for further development, eg in 1-prong decays
- SLD charge-dipole analysis is beautiful, but much room for improvement
- Energy-flow in calorimeter offers hope of including π^0s associated with the heavy flavour decays
- Clear classification of jets as with-lepton or without-lepton can be a powerful tool in sharpening dijet mass resolution
- Residual p_T imbalance in with-lepton vertices can be used to compensate partly for missing neutrinos
- All these tools need tuning with different detector options and assessment using physics examples, in order to make a true evaluation of the importance of any suggested detector enhancements or compromises
    - Meanwhile, experience suggests that one will continue to win rapidly in line with improvements in impact parameter resolution, and redundancy in close-in tracking (eg for optimally handling photon conversions)

Richard Hawkings



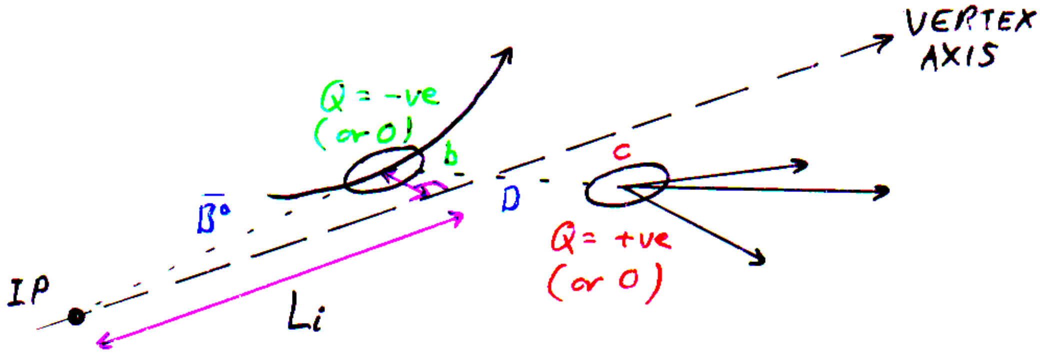


c-tag performance

Dave Jackson

CHARGE DIPOLE TAG

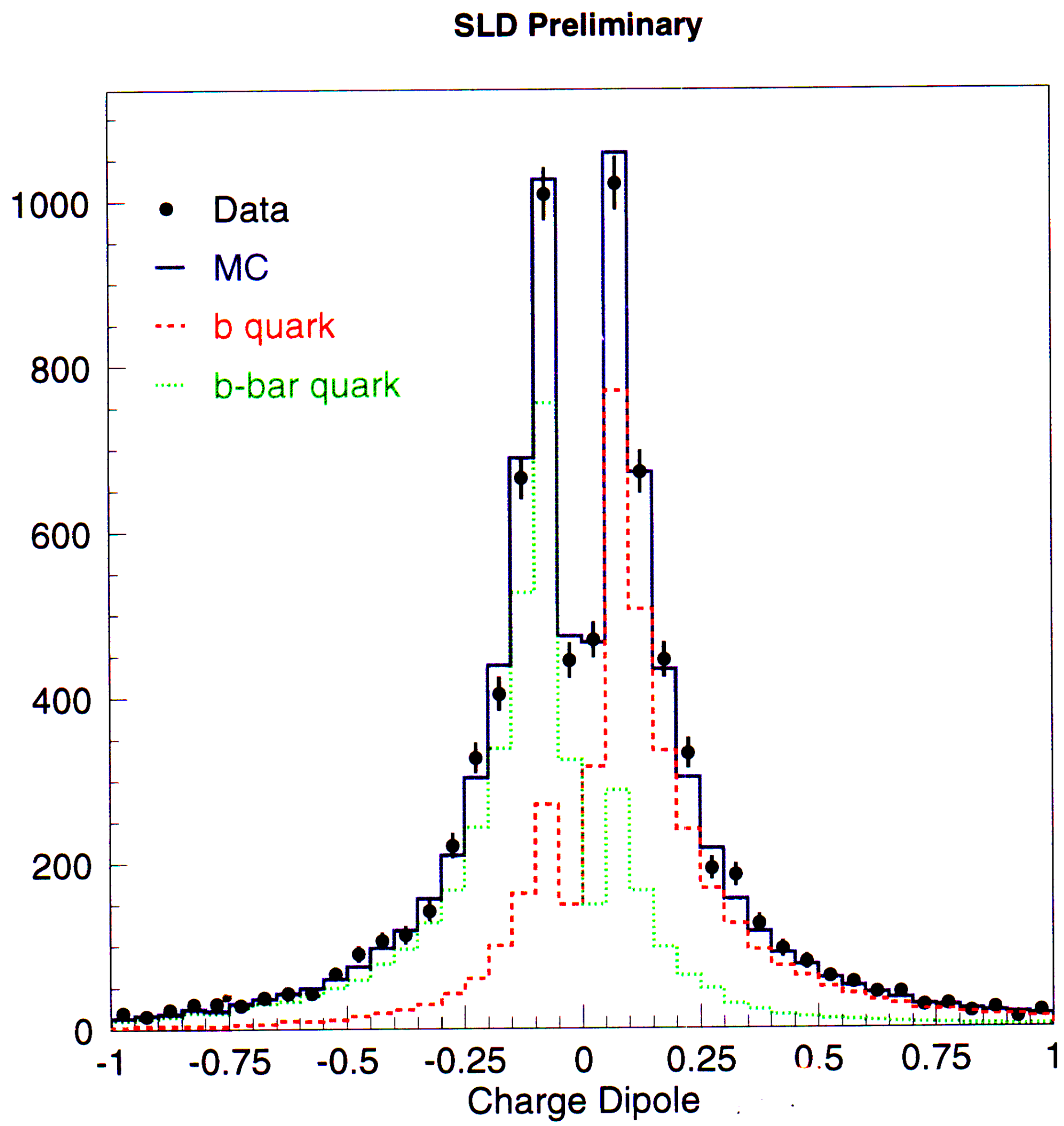
EXPLOIT THE B→D CASCADE CHARGE STRUCTURE



CHARGE DIPOLE; SEPARATE RECONSTRUCTED B DECAY TRACKS INTO CANDIDATE B AND D VERTICES

$$\delta_q = \frac{Q_D - Q_B}{|Q_D - Q_B|} \cdot \mathrm{DIST}\ (B \rightarrow D\ \mathrm{VTX})$$

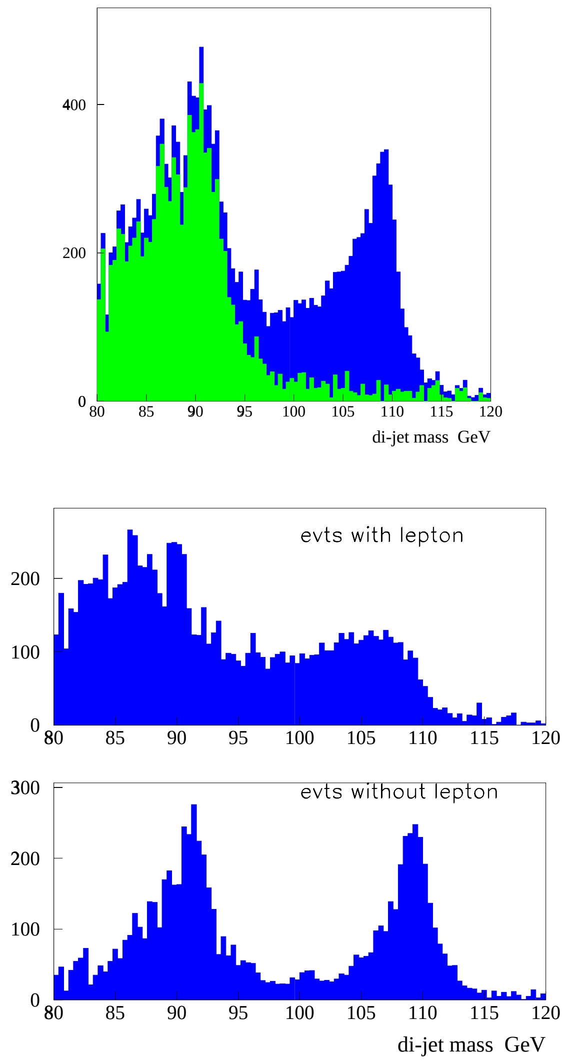
$\delta_q > 0$ TAGS $\bar{B}_s$ DECAY
$\quad\; < 0 \qquad\qquad\quad B_s$



SLD Preliminary
Data
MC
b quark
b-bar quark
0
200
400
600
800
1000
-1
-0.75
-0.5
-0.25
0
0.25
0.5
0.75
1
Charge Dipole

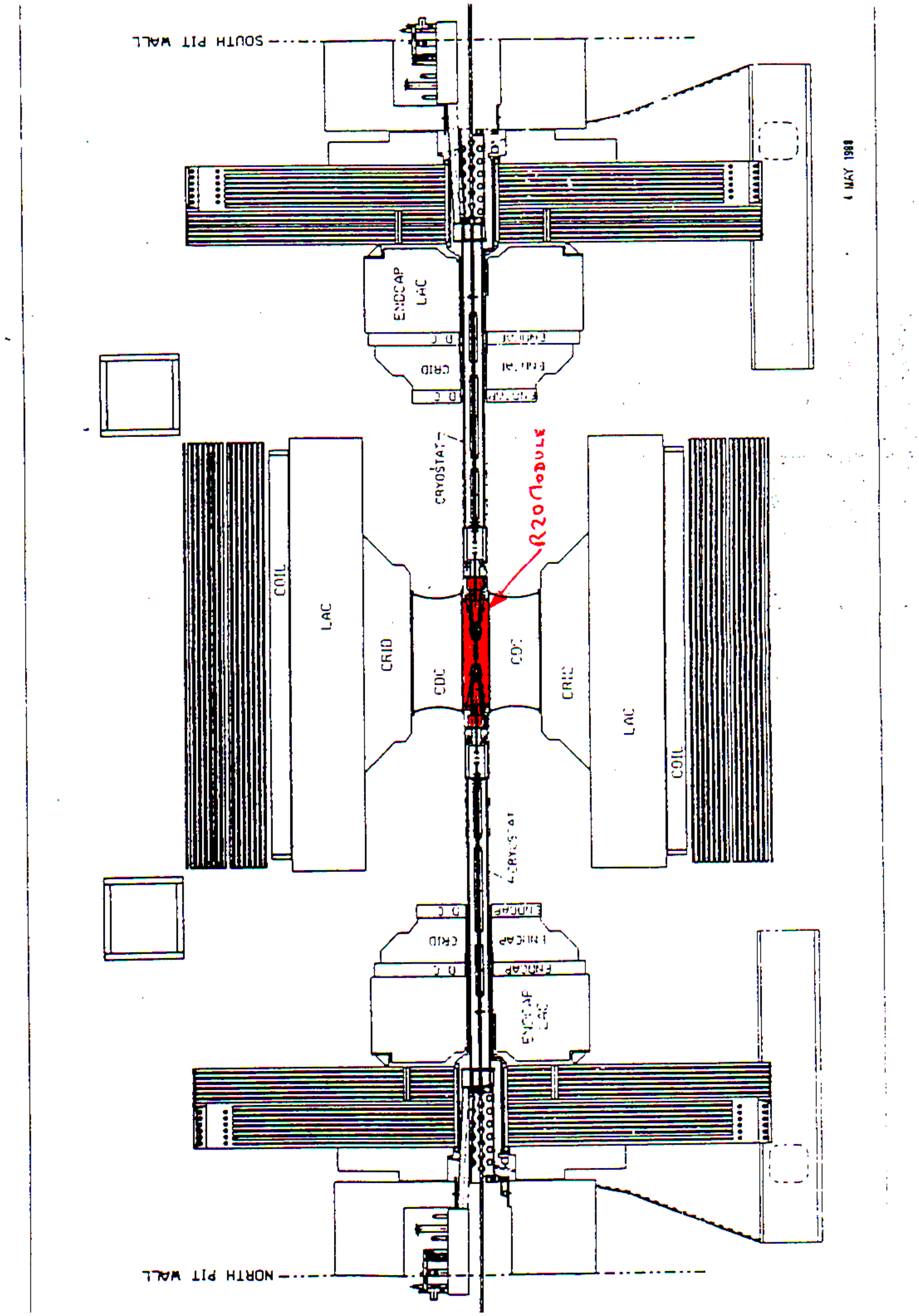
FAST SIMUL.

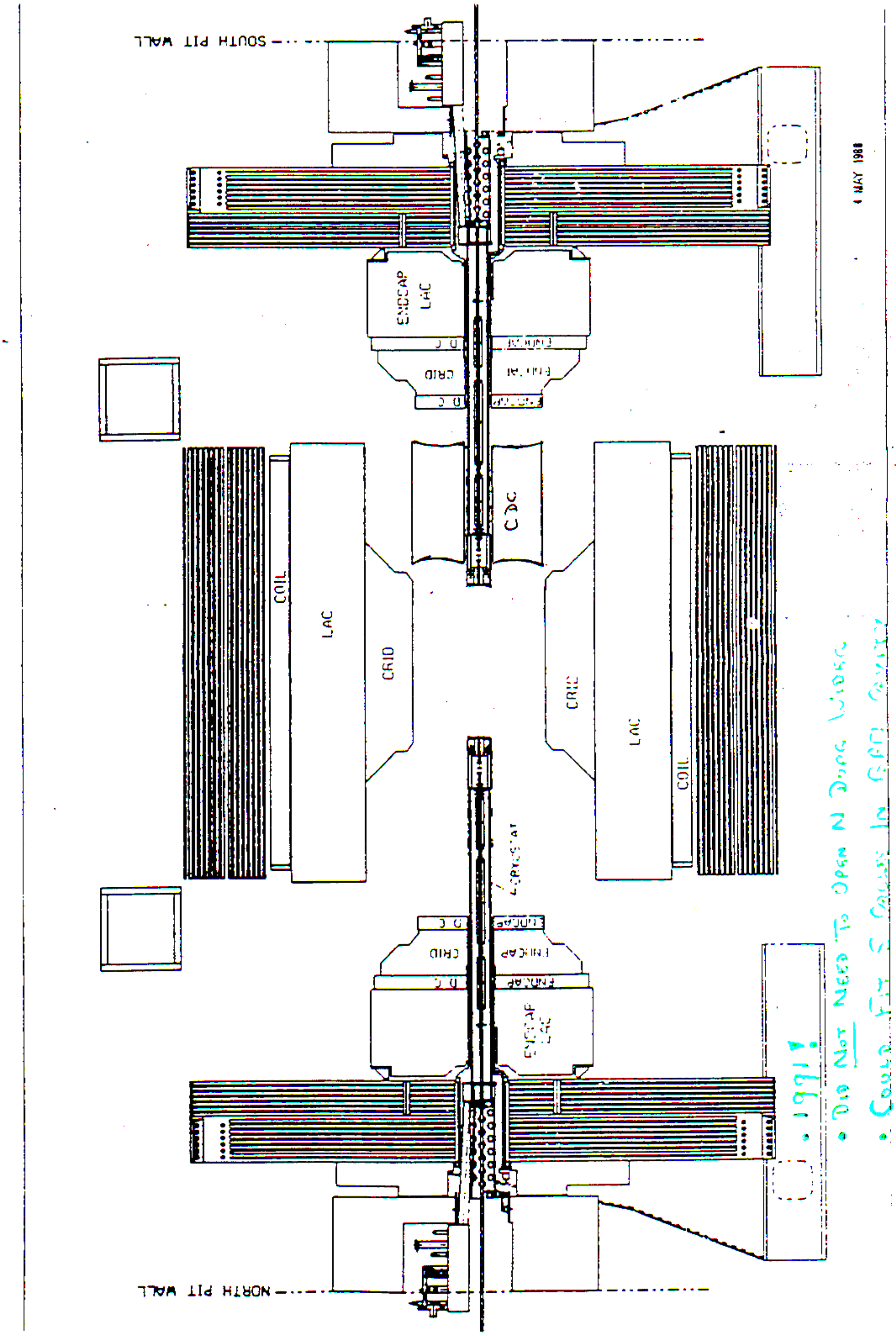
$\sqrt{s} = 500$ GeV, $e^+e^- \rightarrow \nu\bar{\nu}H$ **and** $ZZ \rightarrow \nu\bar{\nu}b\bar{b}$



Conclusions

- We probably have 5 years of R&D before technology choices need to be made
- For all options, important to push hard since there is much scope for development and the physics prizes could be immense
- As usual, the technological developments for vertex detectors are likely to continue to make brisk progress into the distant future (improved pixel detectors are in demand for numerous imaging applications)
- Therefore, vital to ensure convenient access to the inner detector, in order to permit ongoing vertex detector upgrades every few years.
- The preferred technology may well change during the life of the collider.


SOUTH PIT WALL
NORTH PIT WALL
ENDCAP
LAC
CRID
CRYOSTAT
COIL
CDC
R20 Module
4 MAY 1988


SOUTH PIT WALL
NORTH PIT WALL
4 MAY 1988
ENDCAP LAC
CRID
COIL
LAC
CDC
• 1991!
• Did Not Need To Open N Door Wider