

Measurements and Simulation of CPC2-40 CHIP#7 on Motherboard

Initial results from first sample

Brian Hawes Oxford University

January 17th 2006

Mounting of Chip on Motherboard

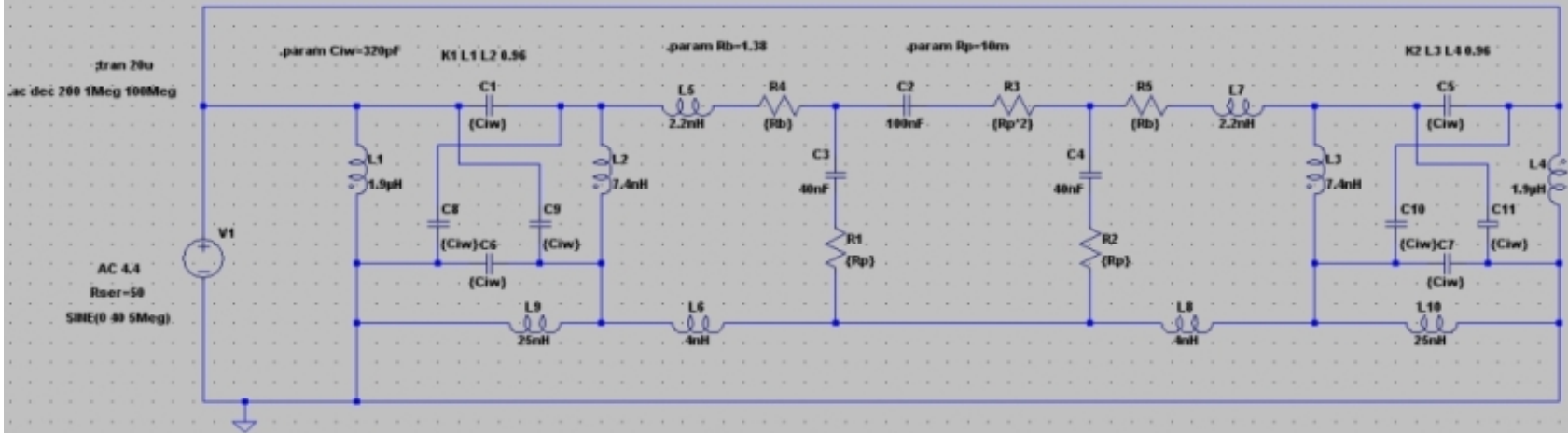
- **The chip supplied is a Single-Metal version, clocked from opposite sides of the array.**
- **The board was designed for a double-metal chip with the two clock planes brought out on adjacent bond pads, on each side.**
- **The careful design of the transformers and transmission-line interconnects was largely nullified by the need to attach wires to the board to re-route the connections.**

Simulation

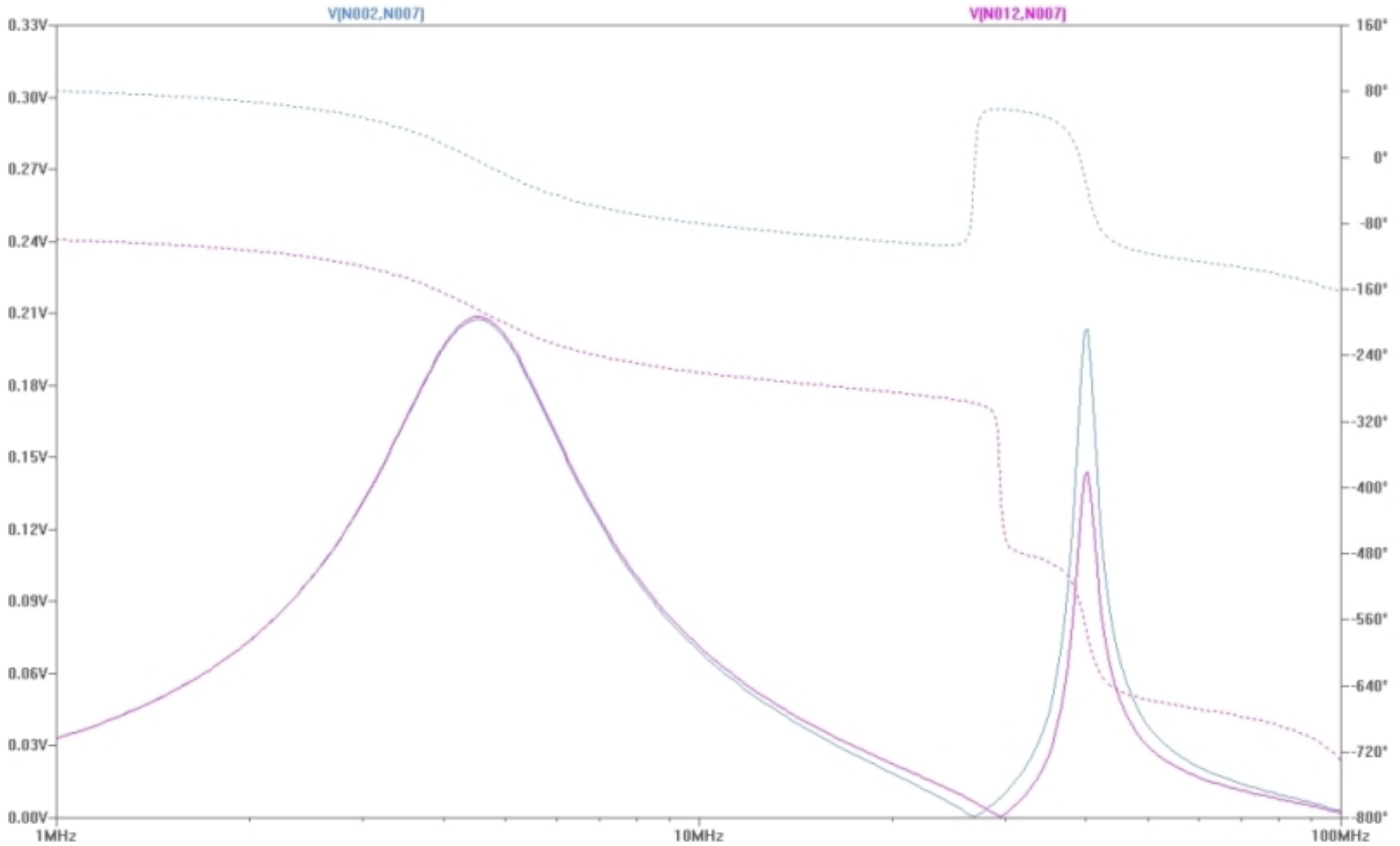
- **An existing SPICE model was modified to match the single-metal chip. This is a simple lumped-constant model, good enough for first evaluations.**
- **Transformer parameters were taken from measurements on prototypes, chip capacitances were taken from Konstantin's notes.**
- **Constructing a model which matches the behaviour of the real circuit enables investigation of parameters such as power dissipation and the effect of changes in parasitic impedances**

Simple SPICE Model

L5/R4 and L7/R5 are bond wire impedances
 L5, L6, L8, L10 are inductances of wires added for single-metal chip
 C1w is representation of transformer inter-winding capacitance



Simulation Results - 1

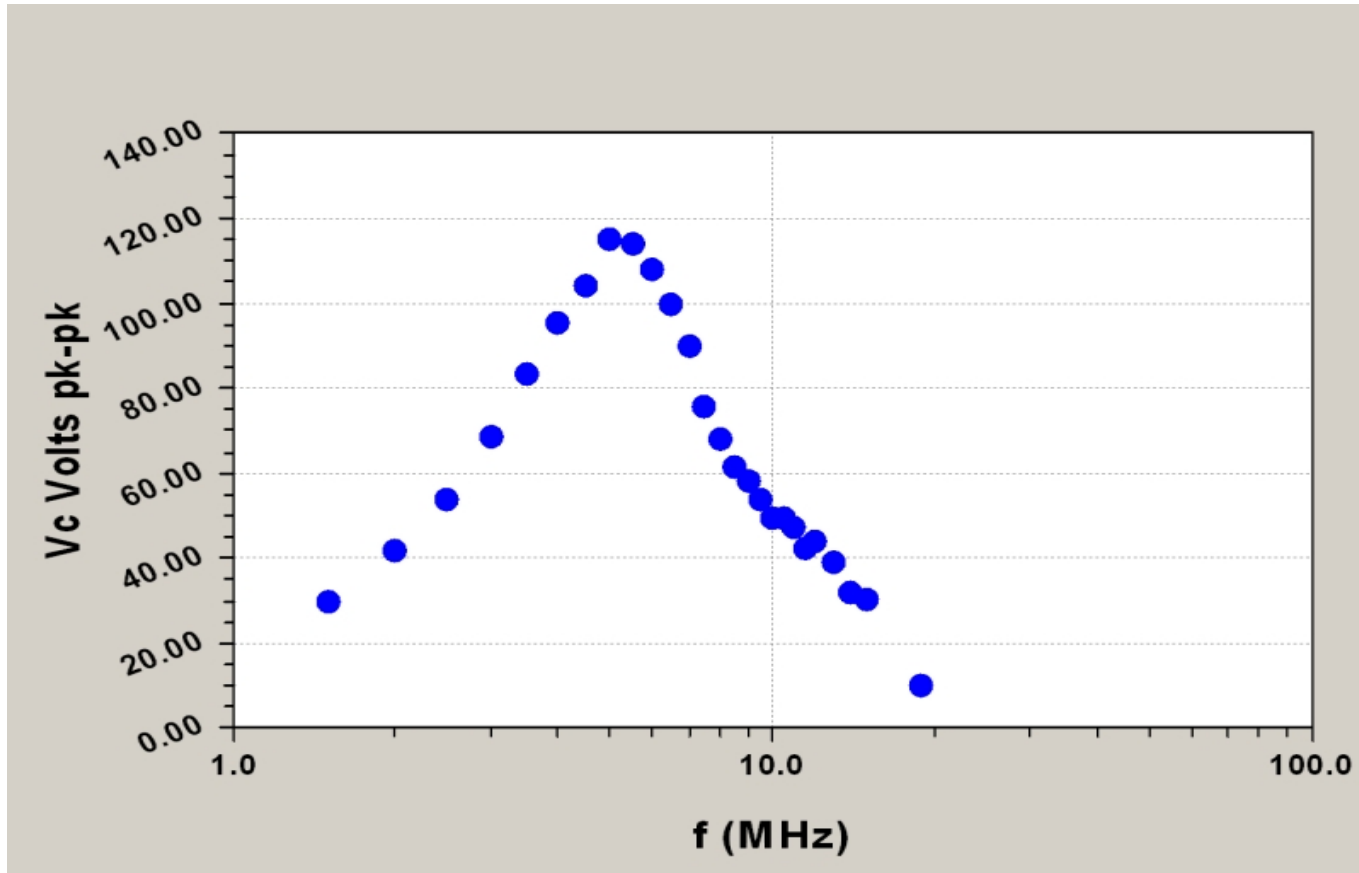


Simulation Results - 2

- **The plot, which is of the voltage from the wirebonds to ground. This can be measured on the board.**
- **The lack of any abrupt phase change near the l.f. peak shows it is not a resonance. It is a convolution of the l.f. roll-off of the transformer and a zero at about 30MHz.**
- **Note that, up to about 30MHz, the two clock signals maintain the correct phase relationship.**

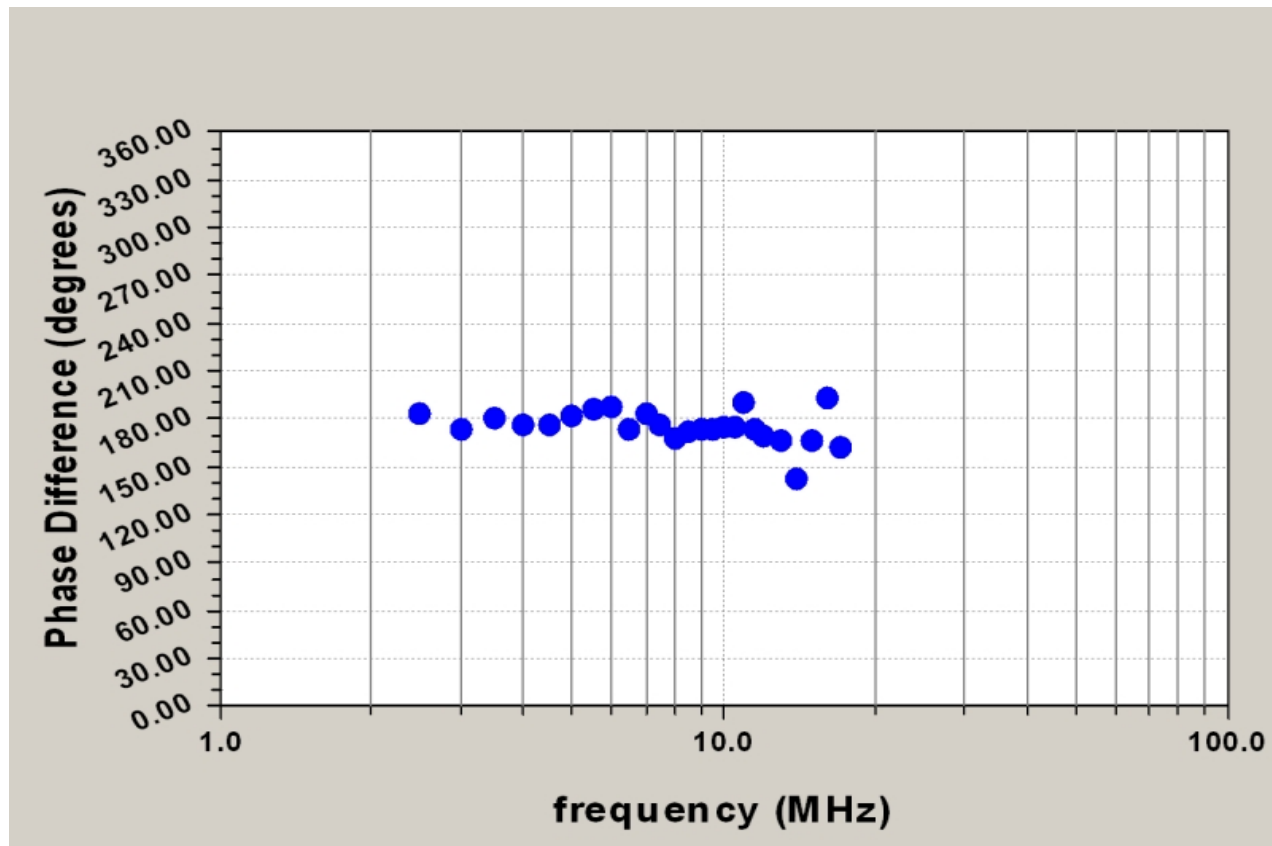
Measurements on the Real Board -1

- This plot shows the measured amplitude response.



Measurements on the Real Board - 2

- This plot is the measured phase difference between the two clocks



Comments on Measured Response

- **The amplitude response is similar to that of the model, which should be no surprise as the model has been adjusted to give best correspondence.**
- **Scatter on the phase measurements at higher frequencies are due to difficulty measuring phase relationship of small signals accurately on an oscilloscope.**
- **We expect delivery of a new R.F. signal generator in February, which will enable better measurements.**

Final Thoughts (for now)

- **We need to measure the clock input capacitance and e.s.r. directly. This will mean removing the bonds to the transformer, but they can be replaced afterwards. Our Agilent LCR meter does not operate above 1MHz but this will still be useful in confirming the model.**
- **By applying a higher voltage, from a lower source impedance. It should be possible to clock the chip from, say, 5Mhz to 15Mhz. The initial tests have all been done with a standard signal generator capable of only 1-volt r.m.s into 50-Ohms**