LCFI Report to the POsC

Konstantin Stefanov

15 February 2008

- WP2: Sensor Design and Production
- WP3: Readout and Drive Electronics
- WP4: External Electronics
- WP5: Integration and Testing

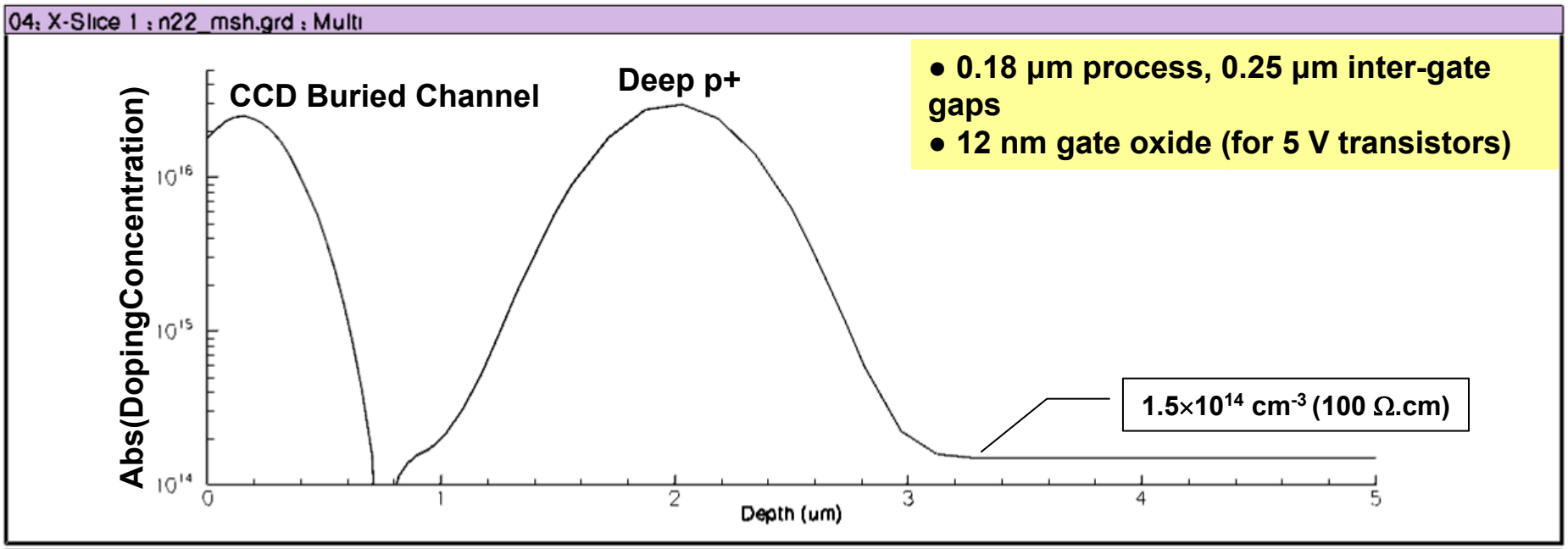
WP2 – Development of ISIS2

- Met on 29 October in the Jazz Semiconductor HQ in Newport Beach, CA
- Development supported by their VP of Technology and Engineering

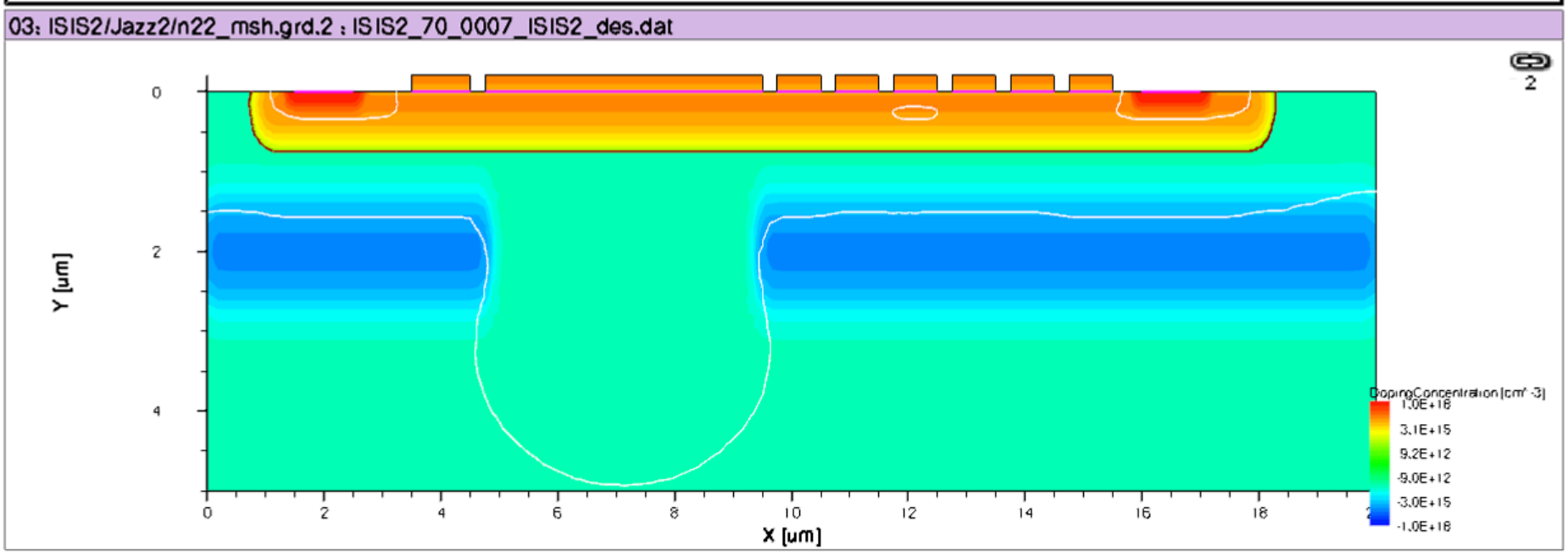
<u>Agreed the following:</u>

- Jazz Semi will develop internally the CCD buried channel implant and the deep p+ implant
  - We will supply custom doping profiles – already done
- The process is 0.18 µm dual gate oxide (1.8 V/5 V)
- Wafers with custom epitaxial layer: 25 µm, ≥100 Ω.cm on p++ substrate
- Will use ¼ of the mask set + 2 additional masks on MPW to reduce costs
- Option to process 5 or 10 wafers, each with process variations, e.g. different doping levels
- Our wafers will be processed independently from the other customers'
- Area = 1 cm^2
- Design is well advanced!
  - 40% complete: pixel layout and logic for row selection done

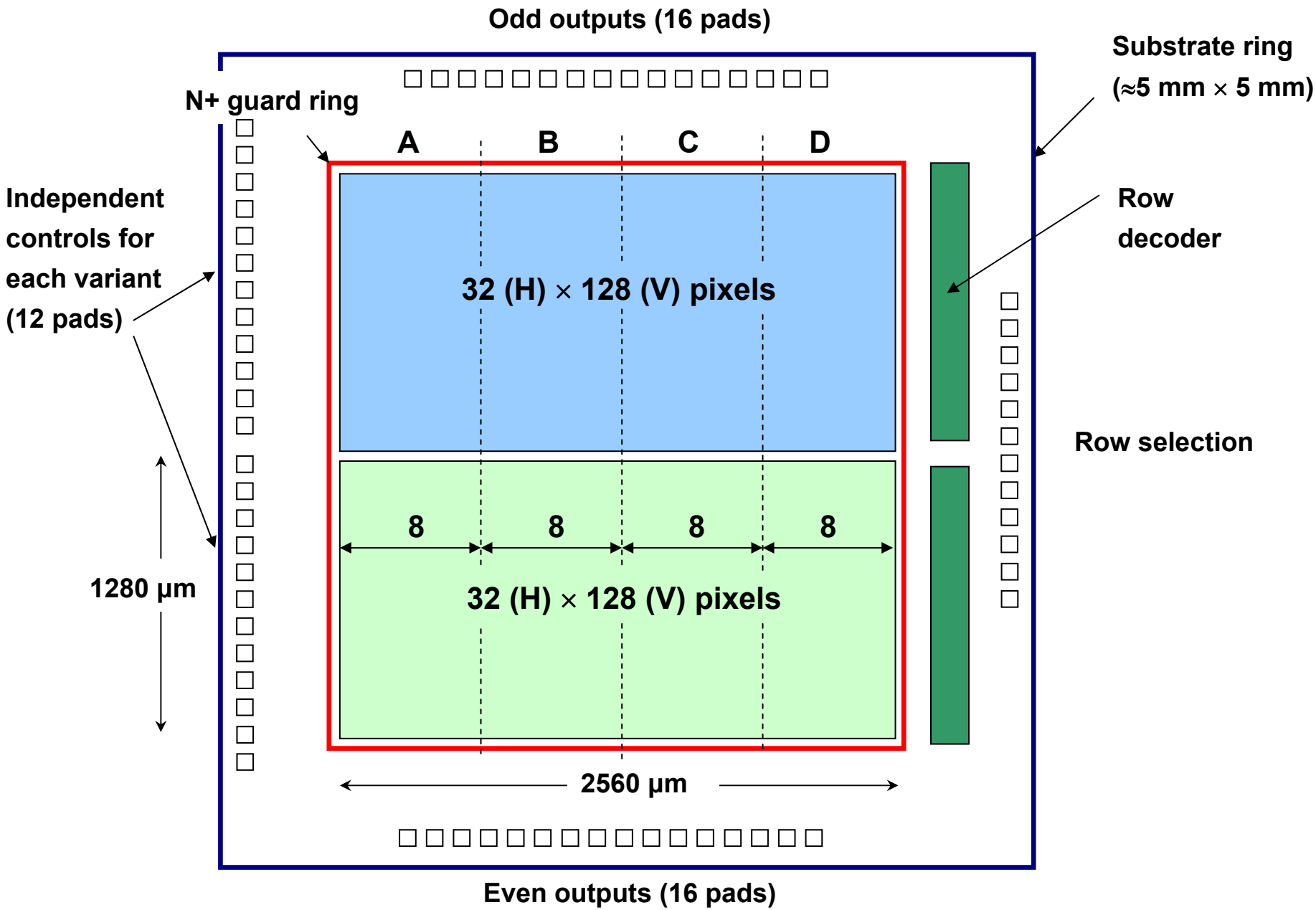
WP2: ISIS2 – Doping Profiles



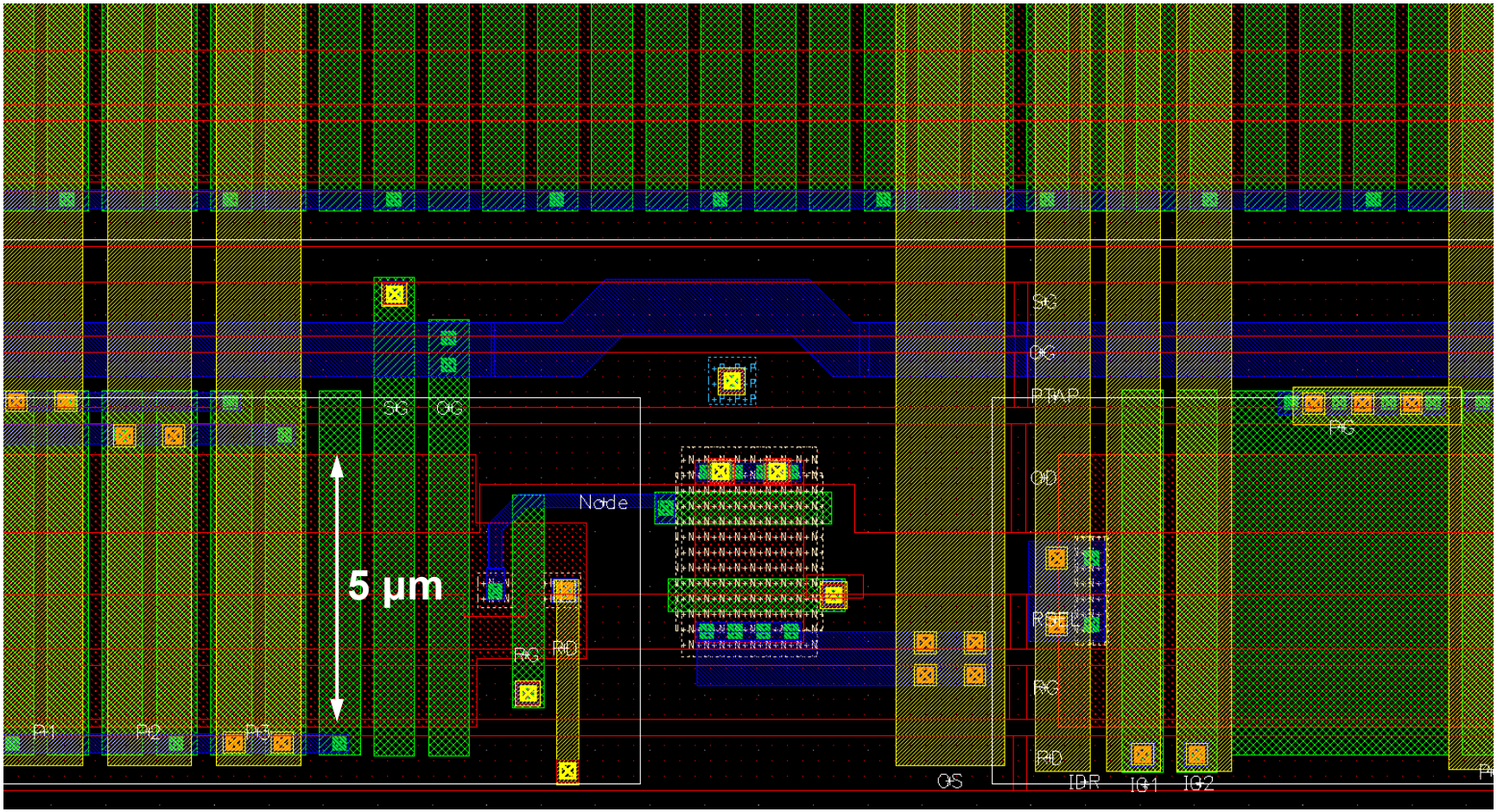
- 0.18 µm process, 0.25 µm inter-gate gaps
- 12 nm gate oxide (for 5 V transistors)



WP2: ISIS2 – Chip Layout

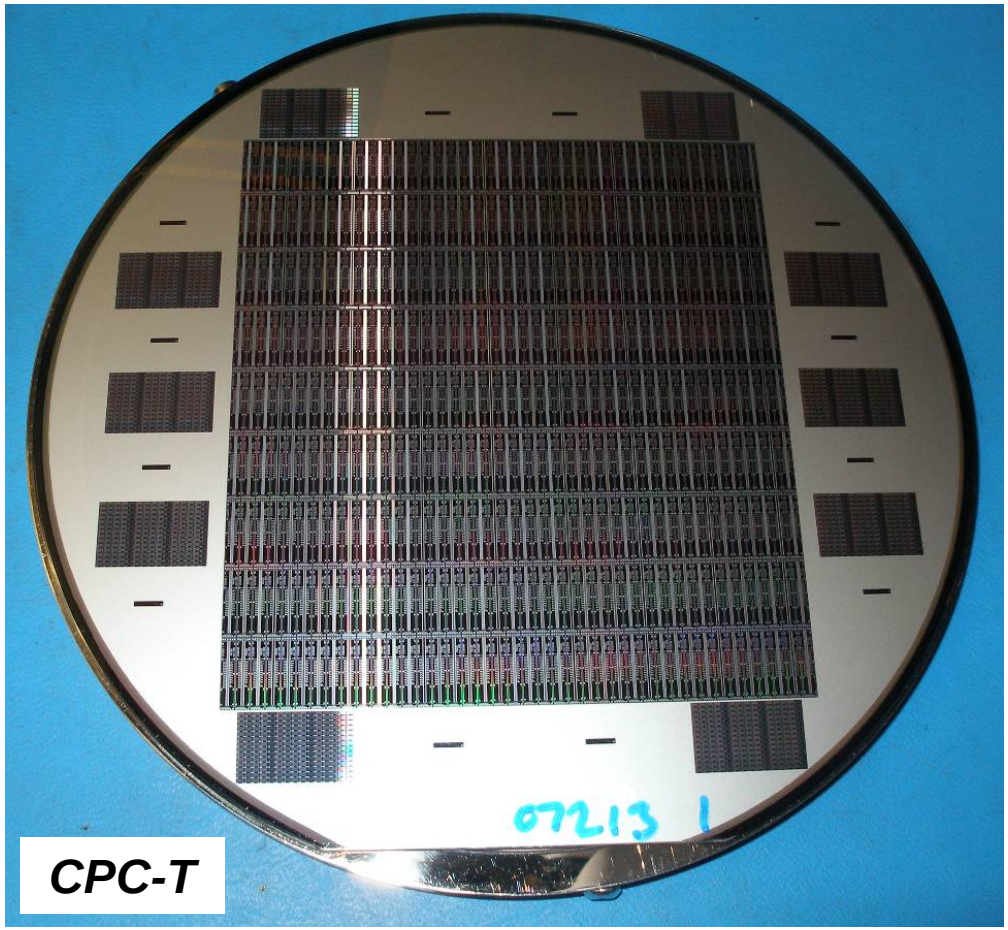


WP2: ISIS2 – Pixel Layout



- 80 µm × 10 µm pixels, 5 µm wide buried channel, 3 metal layers (4 available)
- Consulting with CCD experts from e2v and CMOS image sensor experts from RAL
- Target tape-out date = 8 April 2008

WP2: CPC-T and the last CPC2 (DLM) batch



CPC-T

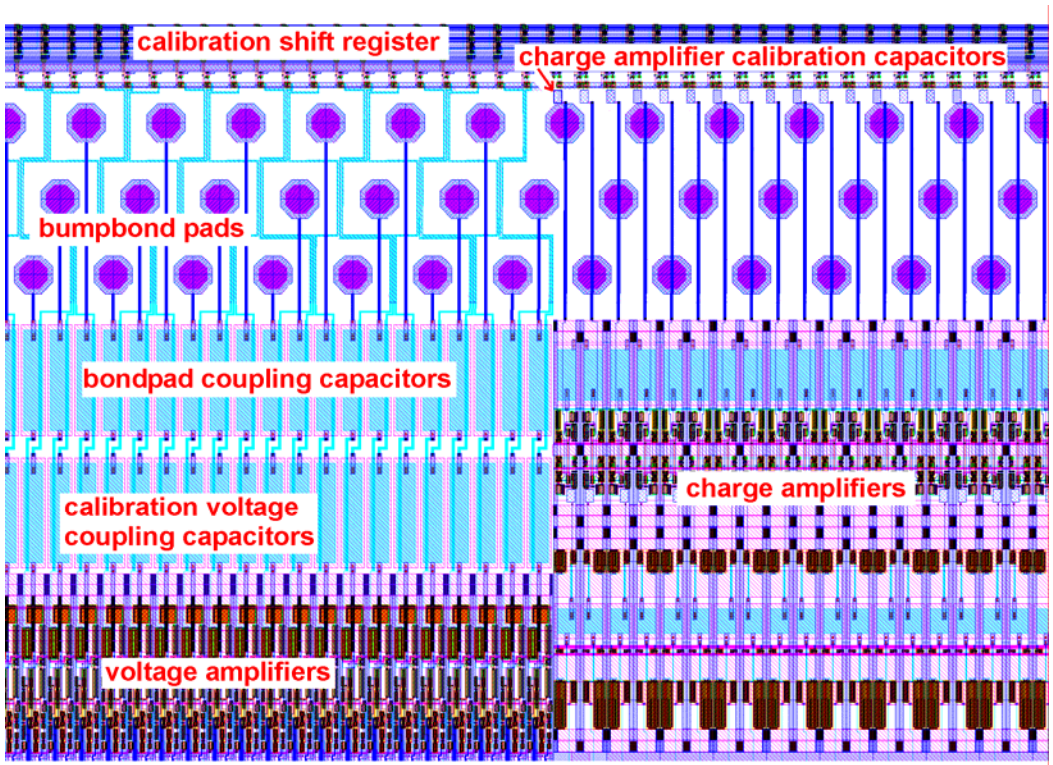
- Wafer manufacture (12 wafers) and DC probing complete
- 360 chips/wafer, 29 different types
- First 6-inch wafers for LCFI
- e2v promised to deliver everything by the end of March

Other work:

- CPC2 (DLM) now in DC probing and testing, delivery imminent
- Four CPC2 wafers in storage at RAL for bump-bonding to CPR2A/B

WP3: CPR2A/B/C

- Three variants: CPR2A, CPR2B and CPR2C submitted in mid-January
- Delivery expected in mid-April
- Major improvements in functionality and performance:
  - ❖ Fully re-designed cluster finder and sparsification circuitry – should cope better with high peak hit densities; added individual column threshold;
  - ❖ Calibration circuit for both charge and voltage channels – allows analogue stand-alone testing of multiple channels;

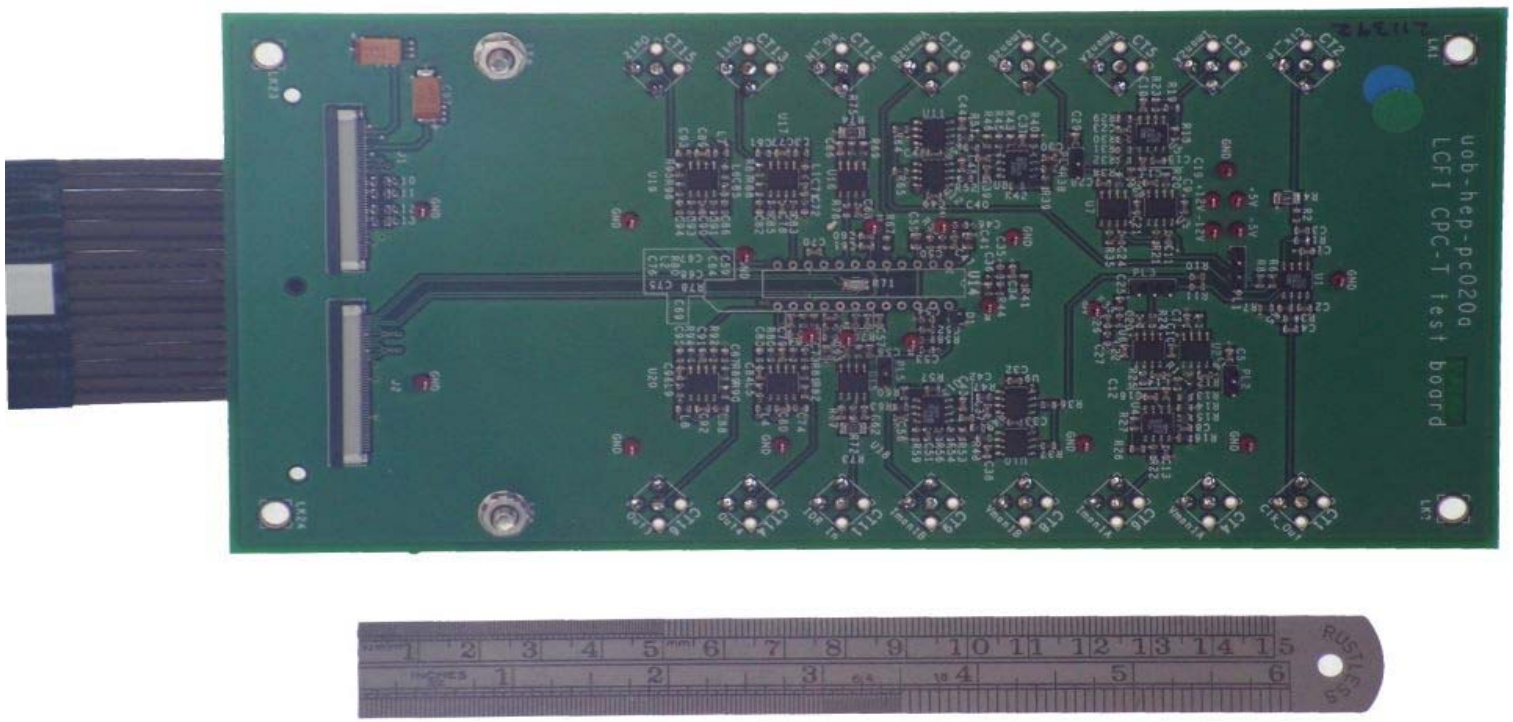


WP3: Readout Electronics

- Other improvements:
  - ❖ Near-constant power supply current in the ADCs (externally controlled) – should reduce interference to the charge channels
  - ❖ Gain matching between voltage channels to per cent level, achieved by lower track resistance and more stable current sources
- Difficulties in simulating the clock distribution and coupling lead us to 3 sub-designs:
  - ❖ CPR2A – clock distribution as in CPR2, but buffer strength is lower, hence lower coupling and interference
  - ❖ CPR2B – no clock buffers (as in CPR1), minimum interference (charge channels worked well in CPR1)
  - ❖ CPR2C – same clock distribution as in CPR2, but only voltage amplifiers (less sensitive to interference, and 250 of them!)
- Testing programme will take ~6 months from April
- After initial testing CPR2A or CPR2B will be bump-bonded to CPC2

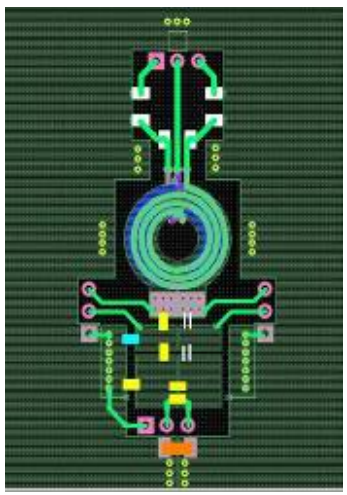
WP4: External Electronics for CPC-T

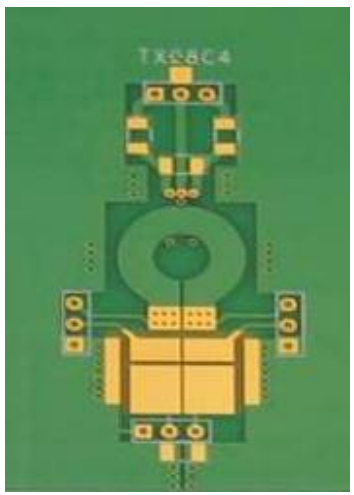
- **CPC-T board :**
  - ❖ **Designed at Bristol (and re-designed due to the package change)**
  - ❖ **Supports clock rates of 50 MHz**
  - ❖ **Provides non-disruptive gate capacitance measurements**
  - ❖ **Fully tested and calibrated**

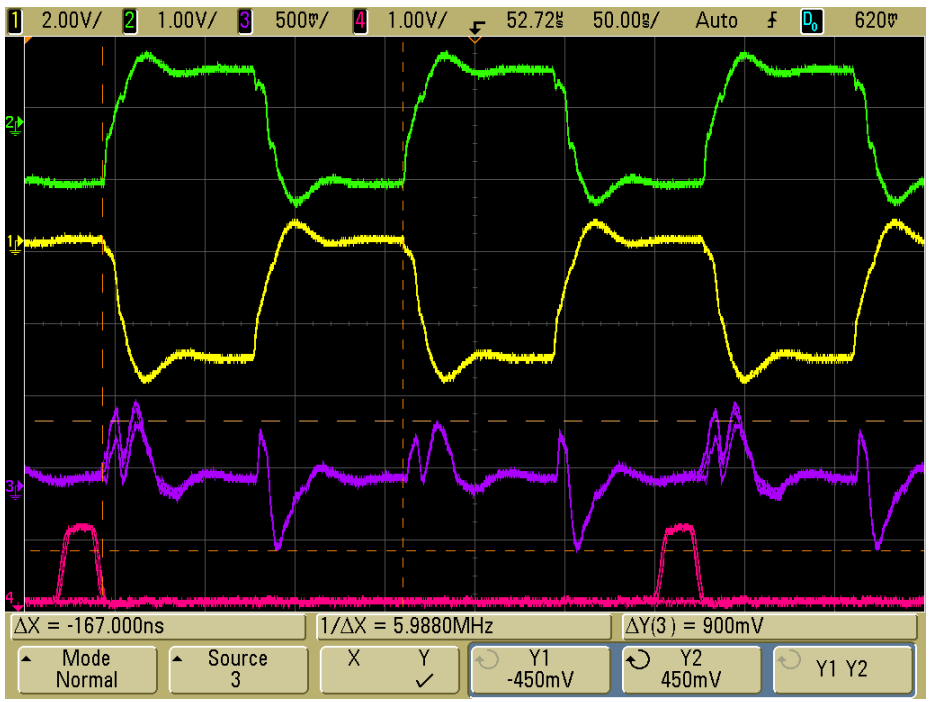


WP4: External Electronics

- New sets of planar transformers :
  - ❖ Improved designs with circular windings for reduced losses
  - ❖ Provisions for serial capacitance – trade-off between current and amplitude
- Studies of the substrate bounce effects in CPC2/CPD1 system
  - ❖ A number of improvements identified, will aim to reach >20 MHz clock operation
- BVM3 – new generation DAQ board in advanced design stage



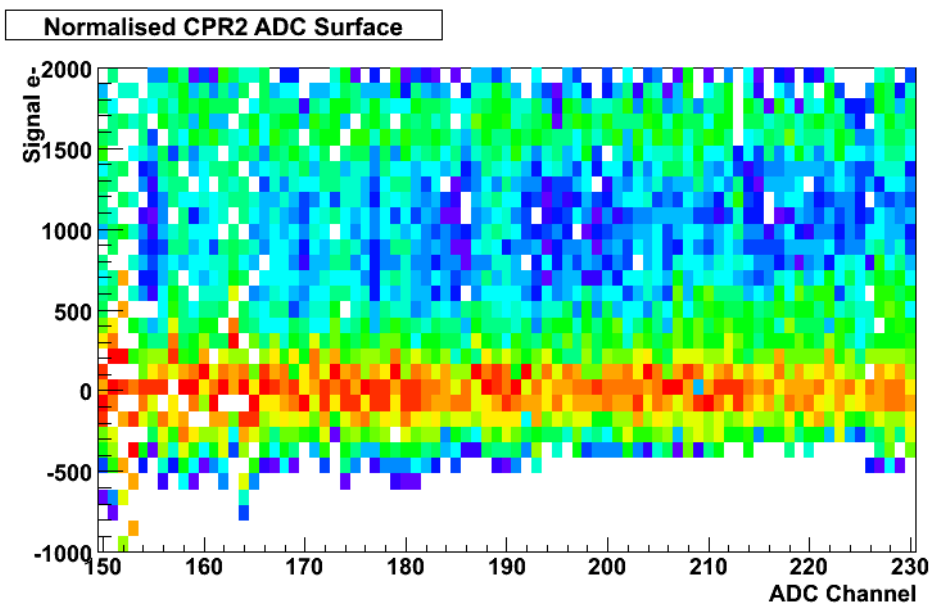


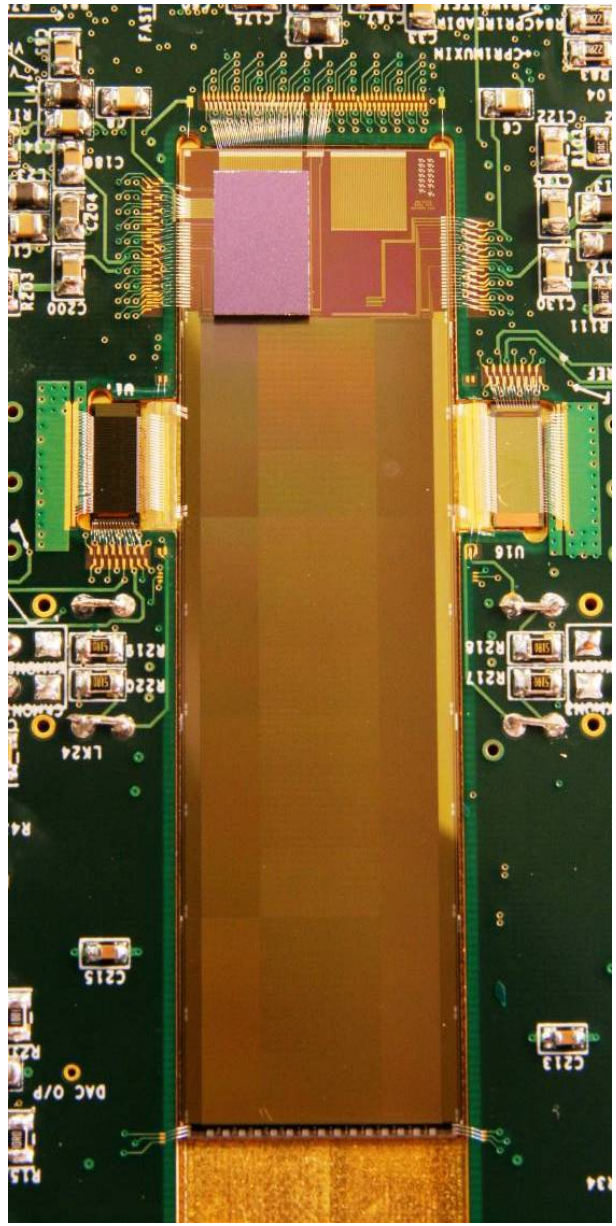


WP5: Testing of Bump-bonded CPC2

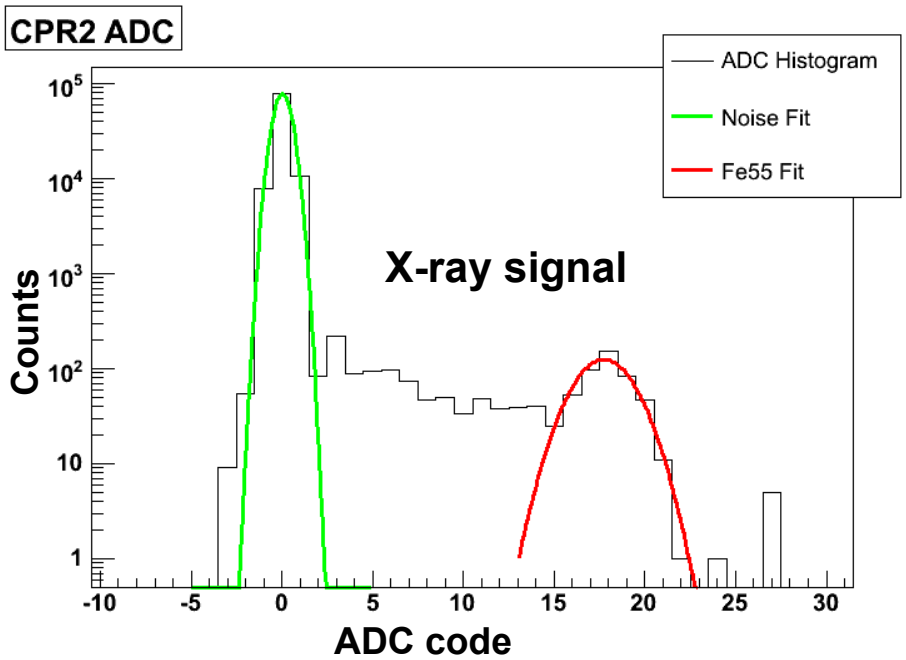
- Testing of the bump-bonded CPC2/CPR2 has completed
  - ❖ Results fully incorporated into CPR2A
- Bump-bonded CPC2-40/CPR2 driven by two CPD1 chips
  - ❖ Works up to 9 MHz
  - ❖ 5 cm long CCD, signals pass 5 “stitches”
  - ❖ Performance of the CPR2 is limiting factor, and gradually deriorates at higher frequencies (missing and/or spurious codes)
  - ❖ Sparse readout (below) up to 6 MHz

➢ Baseline measurements for radiation damage studies (stand-alone CPC1) have been carried out

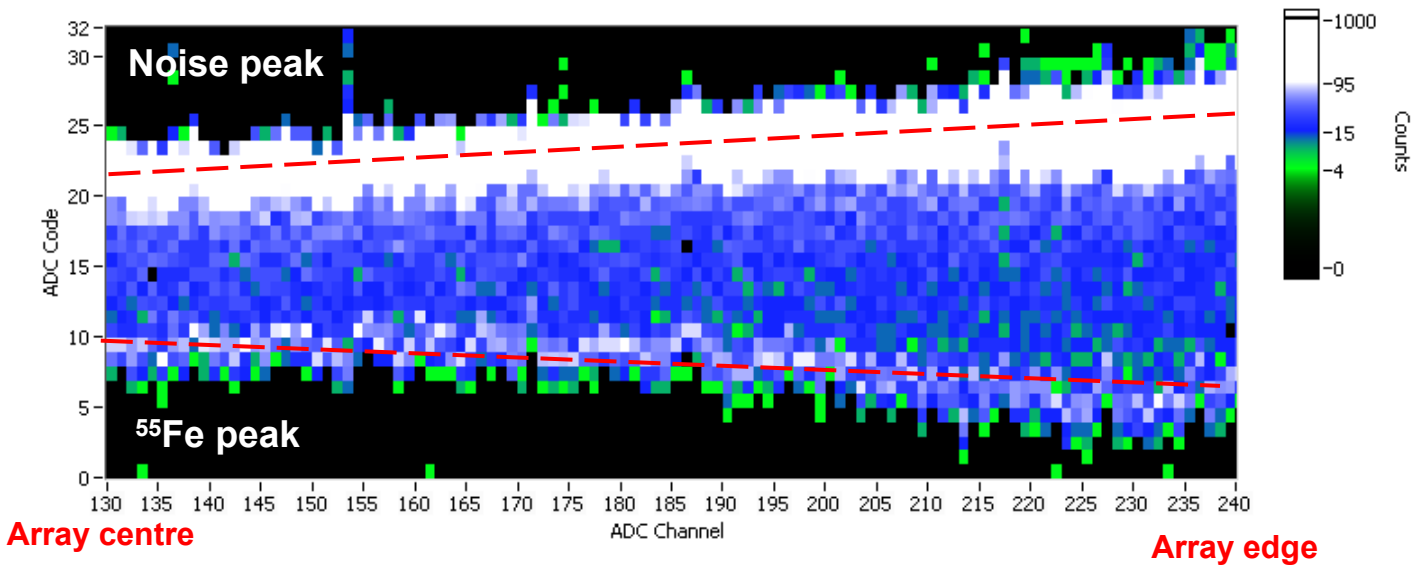




CPR2: Analogue Performance

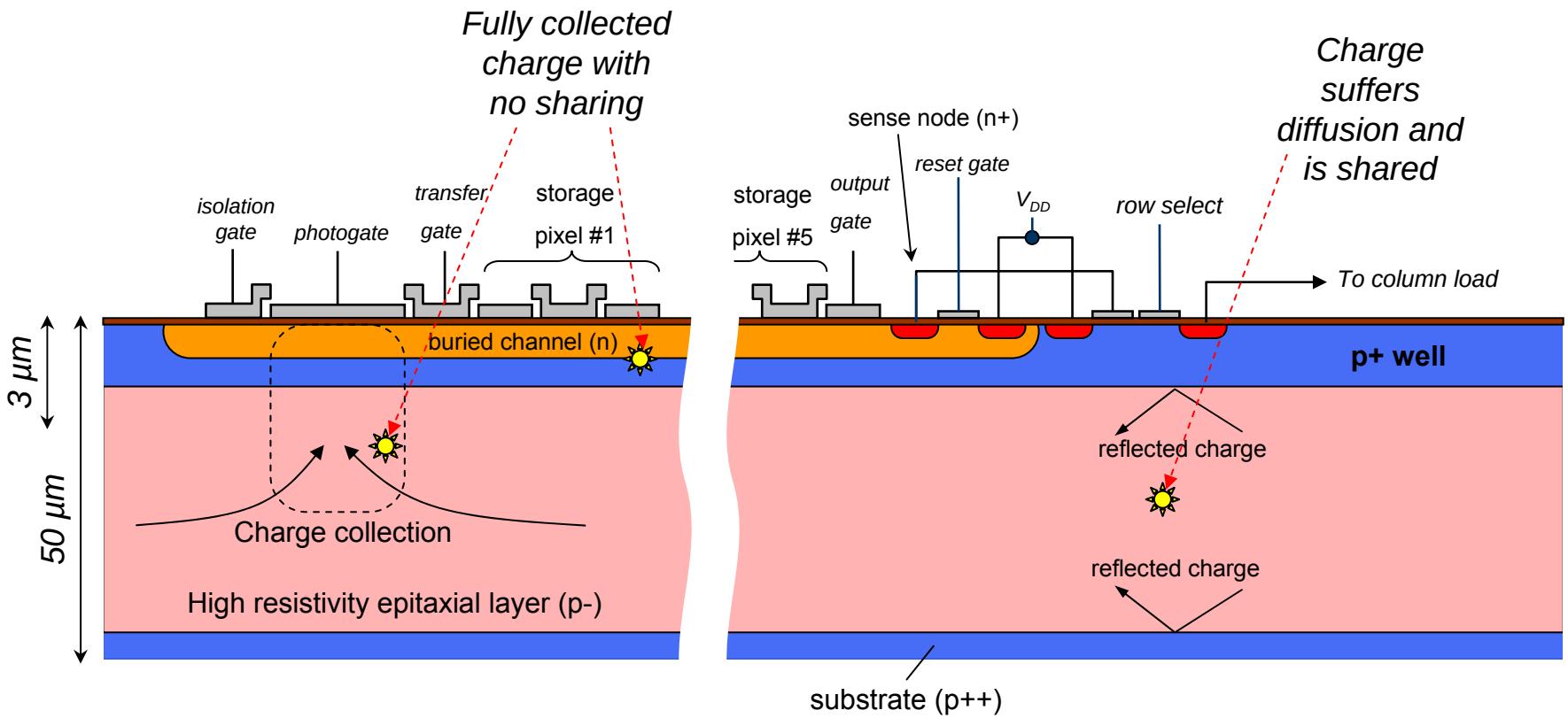


- Signals from all voltage channels observed (here at 2 MHz, 300 mV ADC range)
  - ❖ Gain decreases by 50% away from the chip edges (as in CPR1)
- Noise around 60-80 e-
- Bump bond yield appears to be 100%
- Charge channels did not work – swamped by digital crosstalk from the ADCs

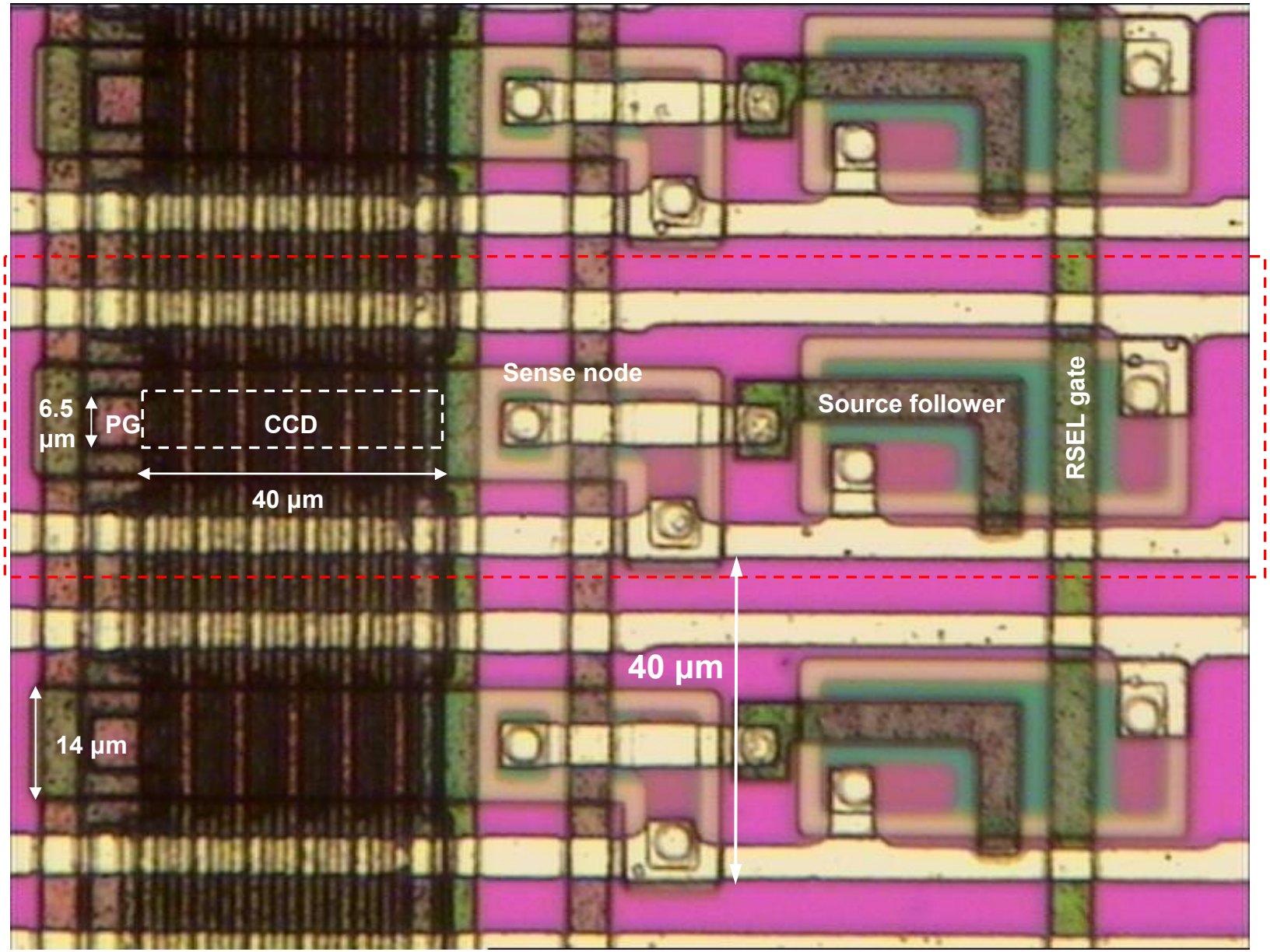


WP5: ISIS1 (p-well)

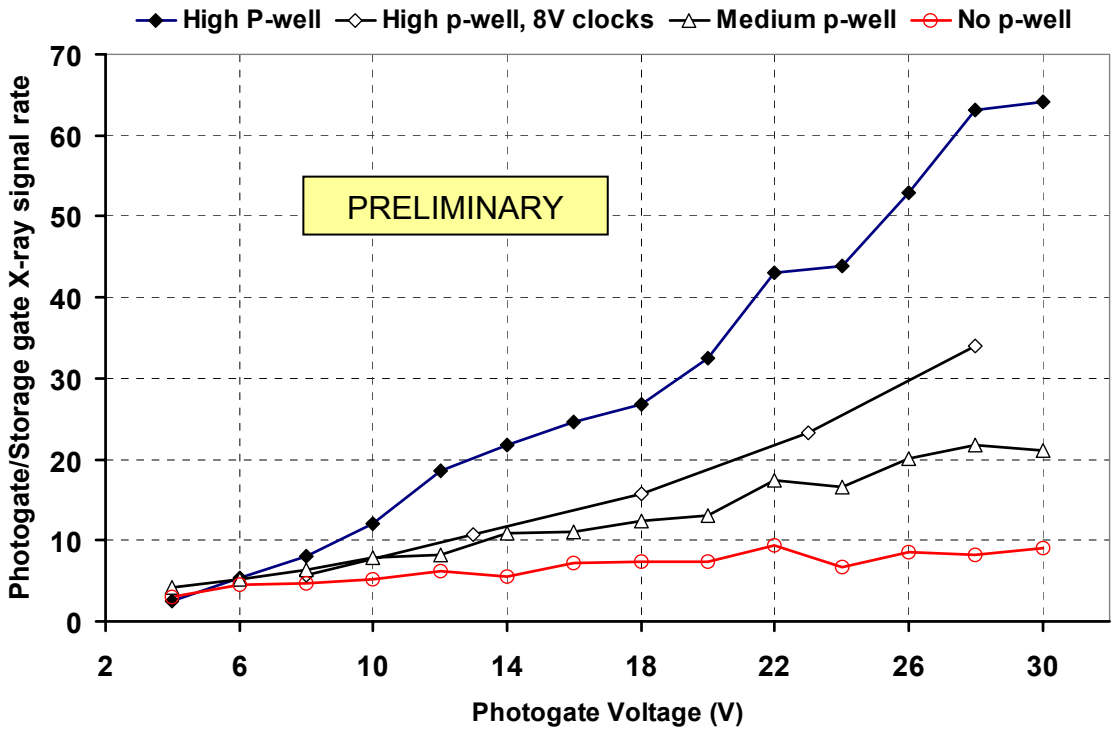
- **In the new, revised p-well ISIS1 we studied :**
  - ❖ **Is the p-well reflecting charge as intended?**
  - ❖ **When and where is the p-well punched through?**
- **Using 5.9 keV X-rays (30 μm attenuation length in Si, converted charge in ≈1 μm sphere)**



WP5: ISIS1 (p-well)



WP5: ISIS1 (p-well)



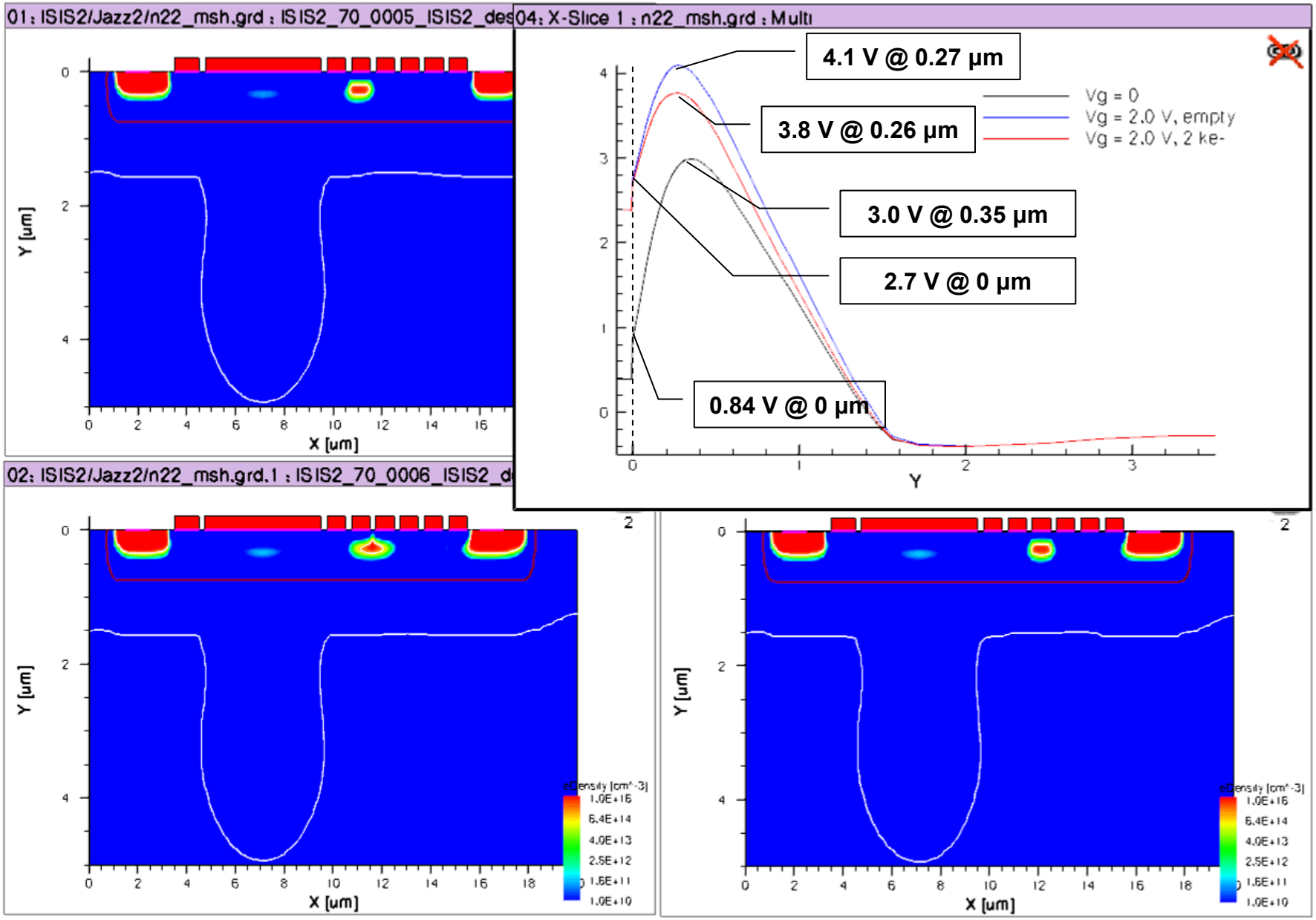
Plotting the ratio *R*:

$$R = \frac{\text{Charge collected on the photogate}}{\text{Charge collected on a storage pixel}}$$

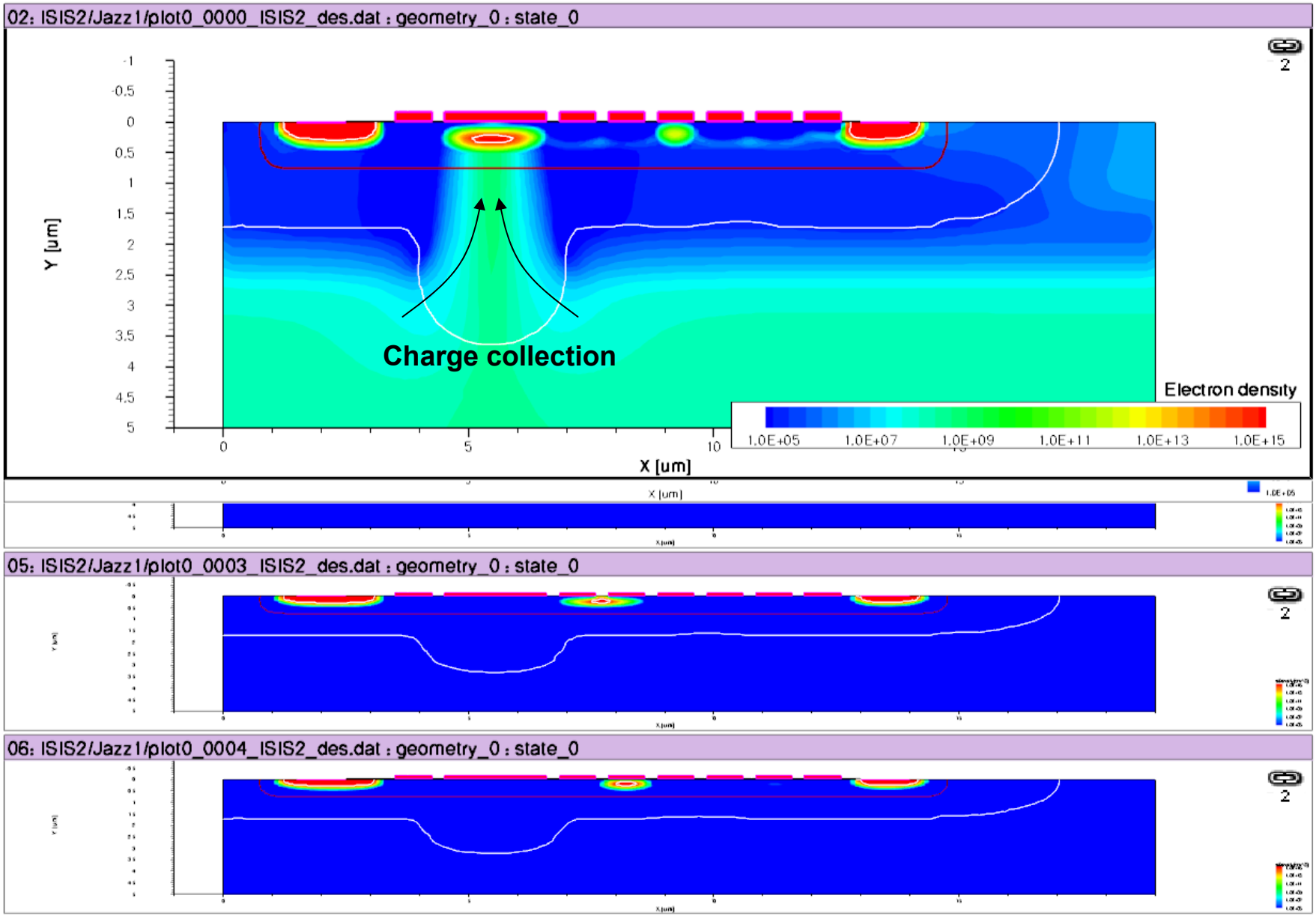
- "High p-well" – good protection of the storage register due to charge reflection
- The p-well works!
  - ❖ The p-well under the storage gates can be punched through by higher clock amplitudes – *R* drops
- Lower ratio with the medium-doped p-well due to lower potential barrier
- "No p-well" – only gate geometry and bias play role, *R* is the lowest
- A paper is in preparation

Thank you

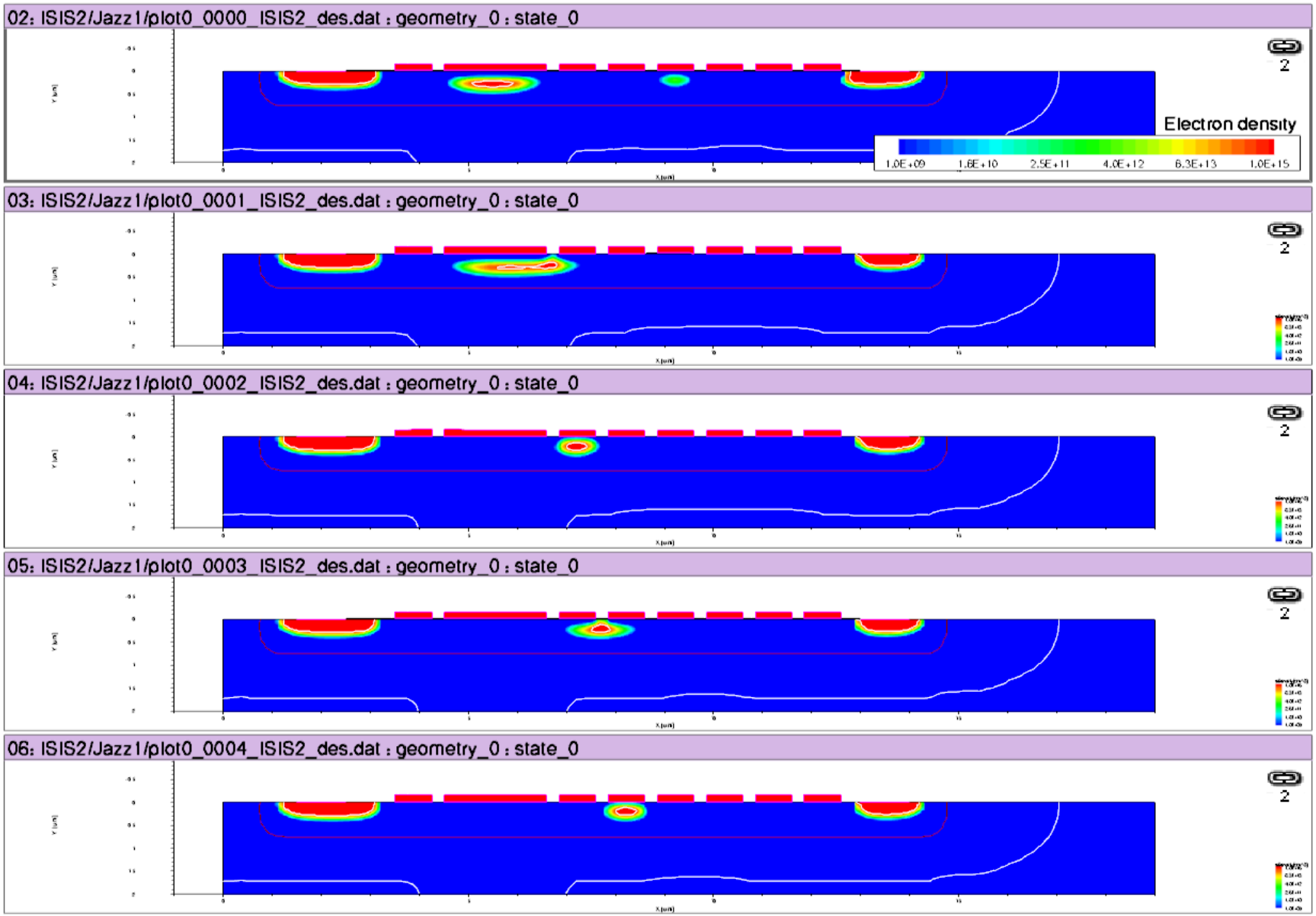
CMOS ISIS2 – Potentials



CMOS ISIS2 – Operation (1)

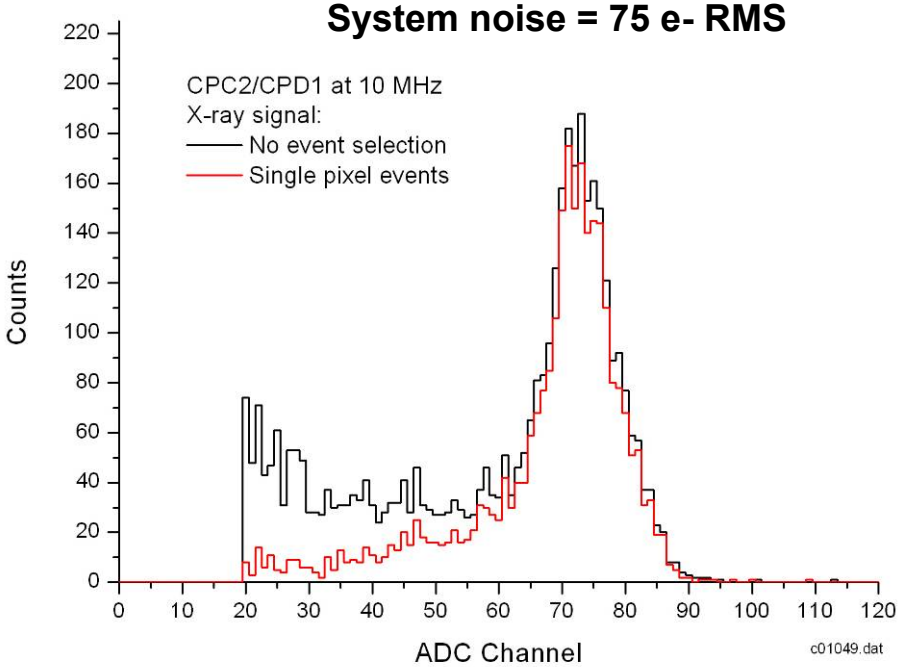


CMOS ISIS2 – Charge Transfer

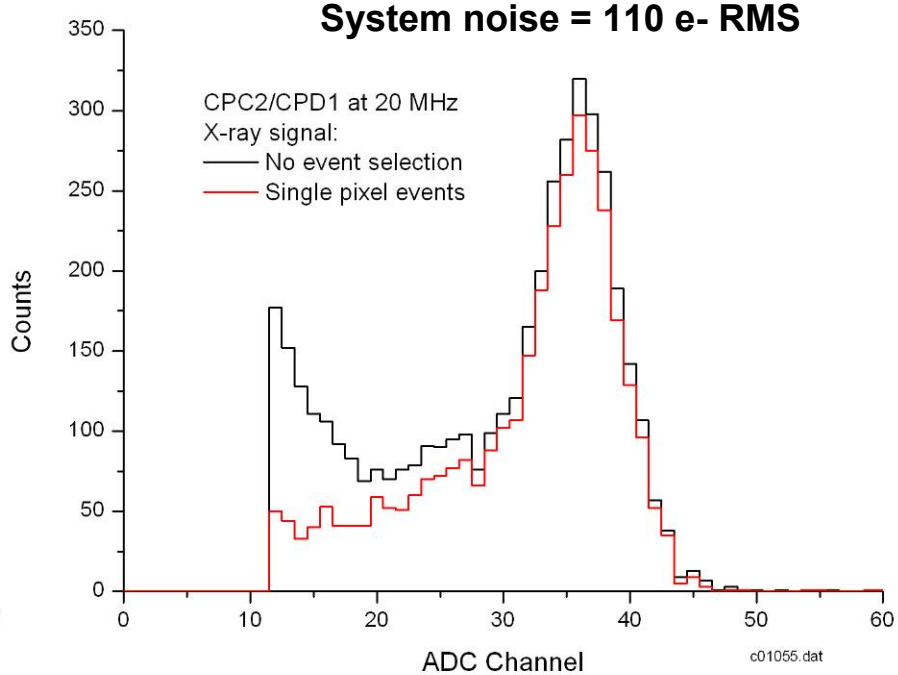


CPC2-10 BLF with CPD1 Clocking

10 MHz
System noise = 75 e- RMS



20 MHz
System noise = 110 e- RMS



- **Stand-alone 2-stage source follower outputs**
- **^{55}Fe signal (1620 electrons, MIP-like)**
- **CPD1 producing clocks in the range 3.3 V to 1.2 V**
- **Noise reduced from 200e- (with transformer drive) to 75 e- (CMOS driver)**
- **CPC2 works with clock amplitude down to 1.35 Vpp**
- **Tests are continuing**

CPR2 Screenshots