Development of HV-CMOS sensors for the HL-LHC upgrade and future experiments

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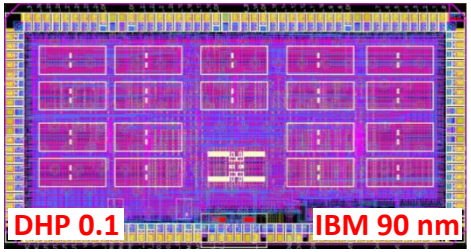
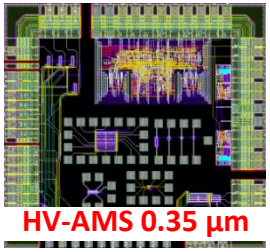
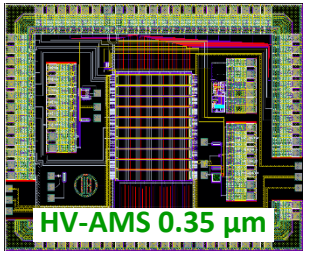
My profile



- **2009** **BSc Electronic Engineering - Uni. Barcelona**

- **2010** **MSc Electronic Engineering - Uni. Barcelona**
  - Readout circuits for DEPFET sensors
  - GAPDs/SPADs/SiPMs in HV-CMOS technologies
  - Belle II and future linear colliders





- **2013** **PhD Engineering and Advanced Technologies - Uni. Barcelona**
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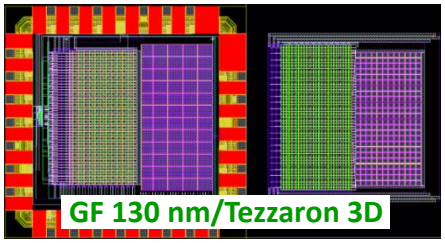
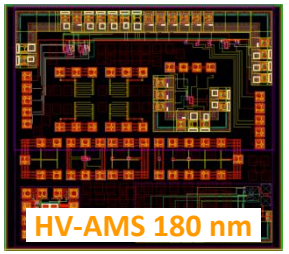
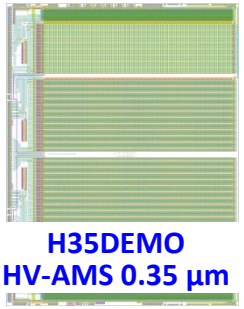
  - Future linear colliders



- **2014** **Short post-doctoral stage - Uni. Barcelona**
  - GAPDs/SPADs/SiPMs in HV-CMOS technologies
  - Biomedical applications

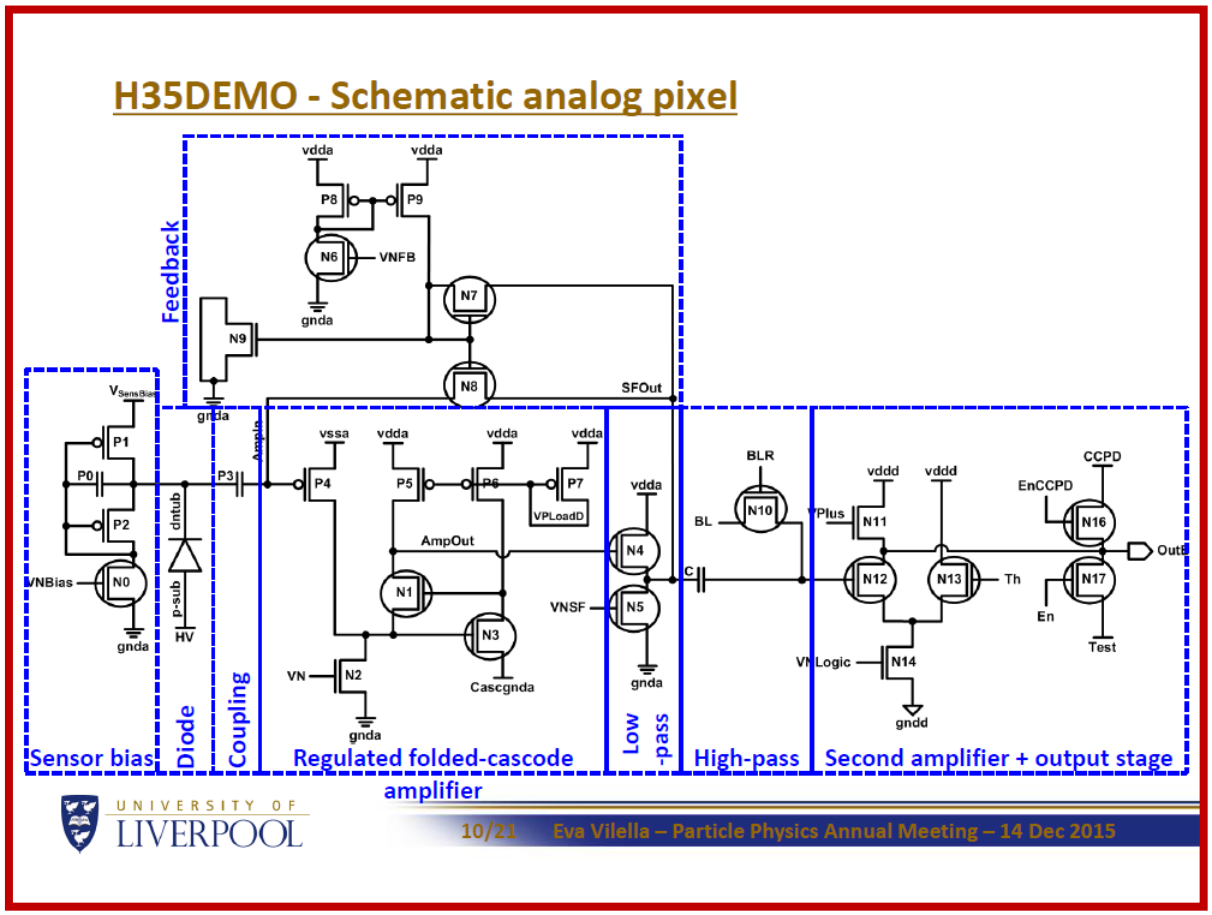




- **Present** **Research associate - Uni. Liverpool**
  - HV-CMOS/HV-MAPS sensors in HV-CMOS technologies
  - ATLAS upgrade, Mu3e and other HEP applications

Why this seminar?

Particle Physics Christmas Meeting 2015 - My slides



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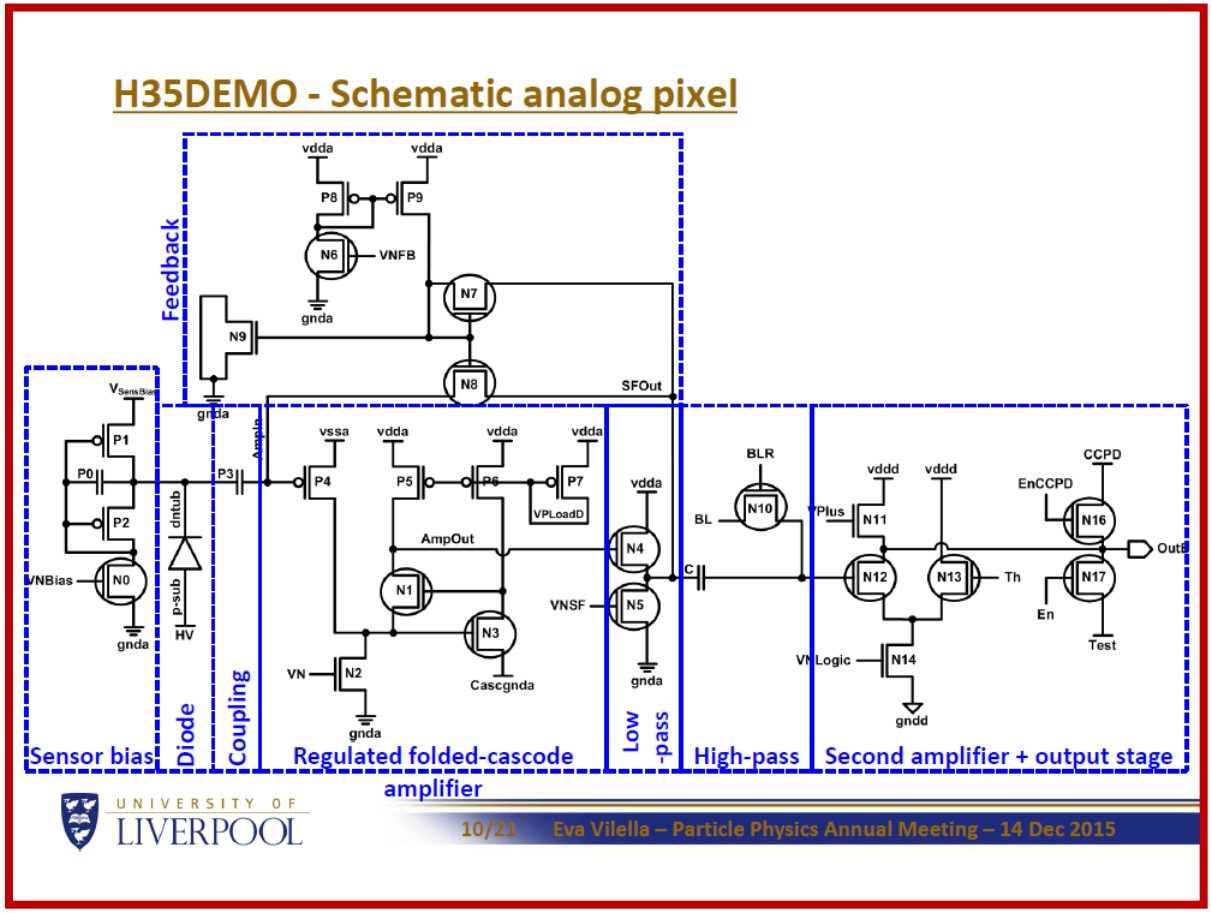

Some of the audience faces

Why this seminar?

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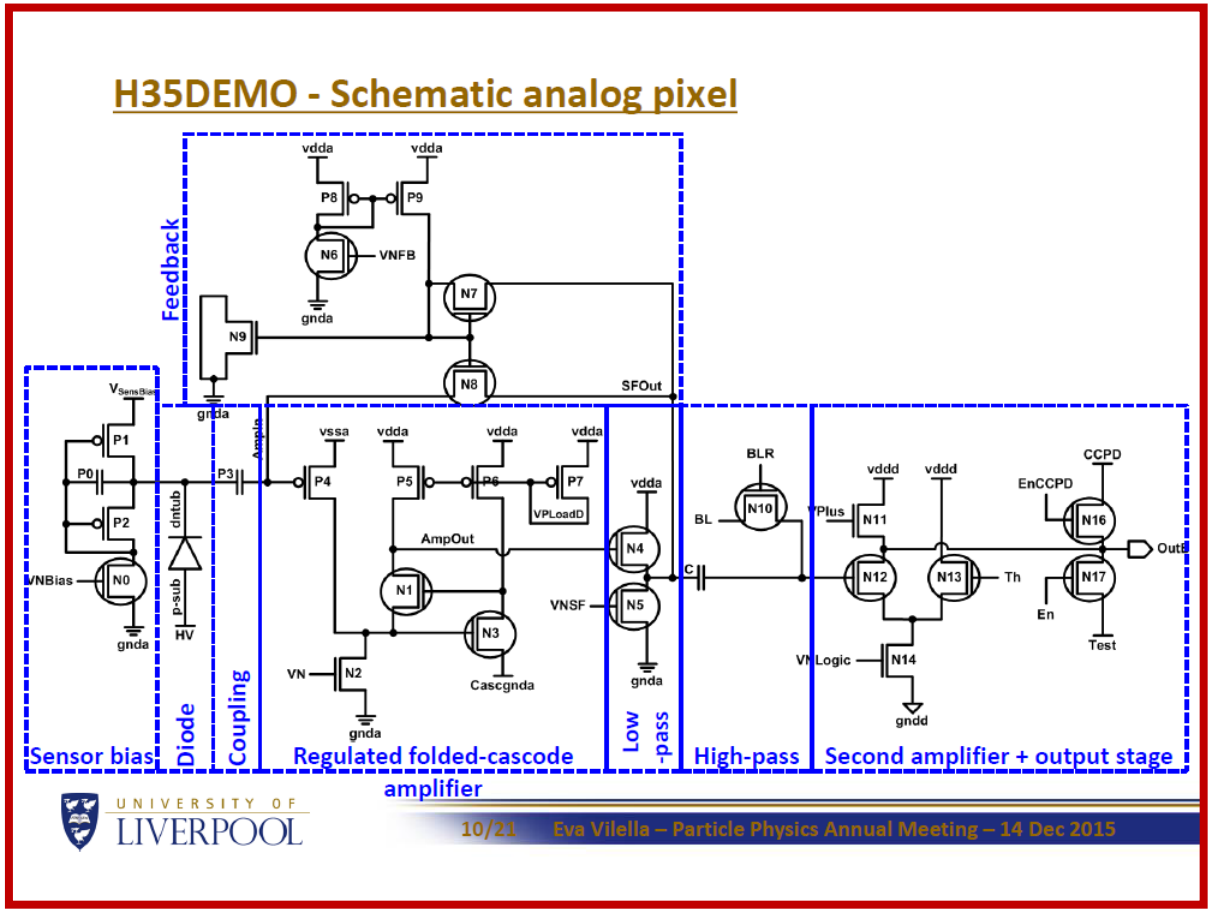


Some of the audience faces

In this Seminar, I will give a general overview of HV-CMOS sensors in easily comprehensible terms to the non-expert

Outline

1. **CMOS sensors**
   - Technology details
   - HEP applications
   - Practical advantages
   - Future HEP experiments
2. **HV-CMOS/HV-MAPS sensors**
   - Technology details
   - Available foundries
   - HV-CMOS developments
3. **HV-CMOS development at Uni. Liverpool**
   - H35DEMO prototype. Design and first measurements.
   - TCAD simulations
   - New prototype
4. **Conclusion**

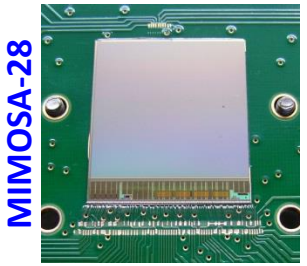
CMOS sensors

- **Innovation** → Amplification integrated in each pixel
- **Application in photonics:**
  - 1993 → First application for photography
  - Currently leading sensors in the imaging field
  - Main application in mobile phones and digital cameras
- **Application in HEP:**
  - 1999 → First proposal for HEP
  - **MAPS = Monolithic Active Pixel Sensor**
  - MAPS development by many different institutes:

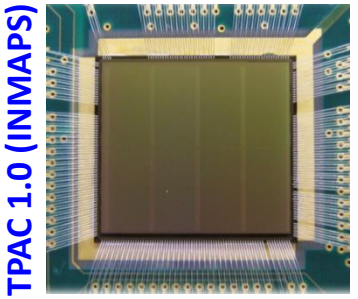
Detector name	Institute
MIMOSA family (>30 prototypes!!) (*)	Uni. Strasbourg - IPHC
DNW MAPS	INFN
INMAPS	RAL, CERN

(*) http://www.iphc.cnrs.fr/List-of-MIMOSA-chips.html

Resolution-crazy camera prototype by Canon (250M CMOS pixels) Sep. 2015

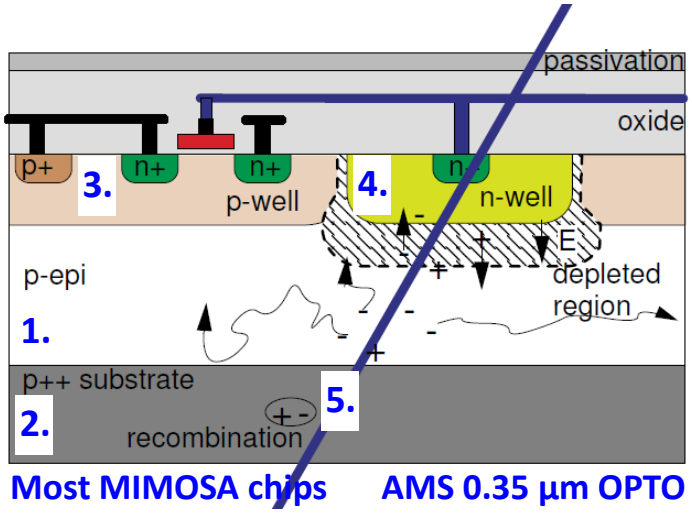


MIMOSA-28

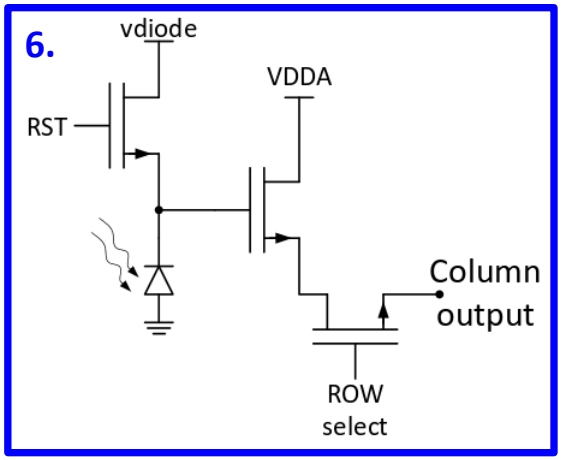


TPAC 1.0 (INMAPS)

MAPS sensors - Technology details



Most MIMOSA chips AMS 0.35 µm OPTO



Pixel = sensing diode + amplifier to buffer the signal

1. Lightly doped p-type **epitaxial layer (~14-20 µm, active volume)**

→ Not fully depleted as CMOS technologies support LV only

→ **Charge collection mainly by diffusion (<100 ns)**

→ 100% fill-factor

2. Highly doped p-type Si-substrate

3. P-well implantation (bulk of nMOS transistors)

4. N-well implantation (collecting electrode)

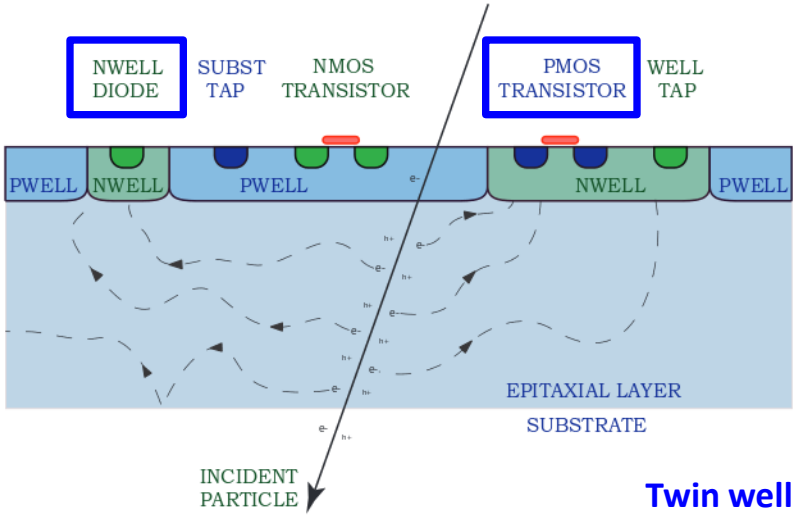
5. MIPs produce **80 e^-/h^+ pairs per µm (~1000 e^- per event)**

6. Only nMOS transistors are possible in the pixel area (twin well)

→ Very simple in-pixel amplifier (3T cell)

- More complex electronics at the periphery of the sensing matrix
- Fabricated in commercial CMOS technologies (leading edge performance, low-cost)

MAPS sensors - Technology details



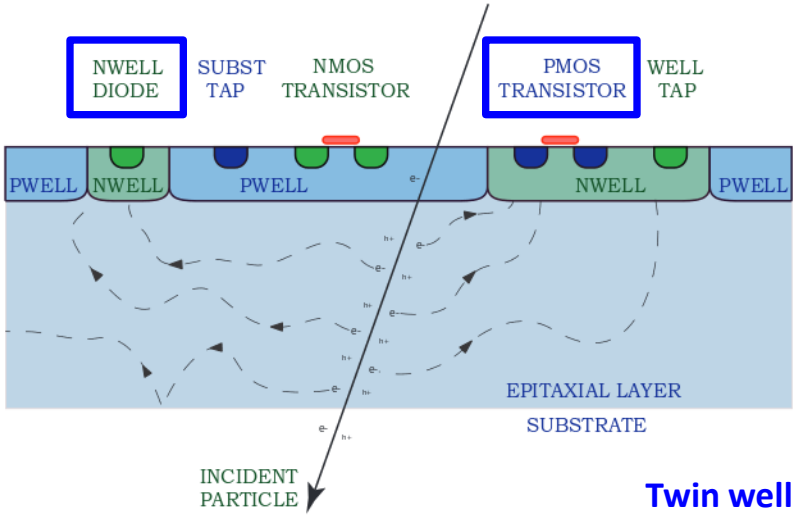
Twin well

MAPS limitations:

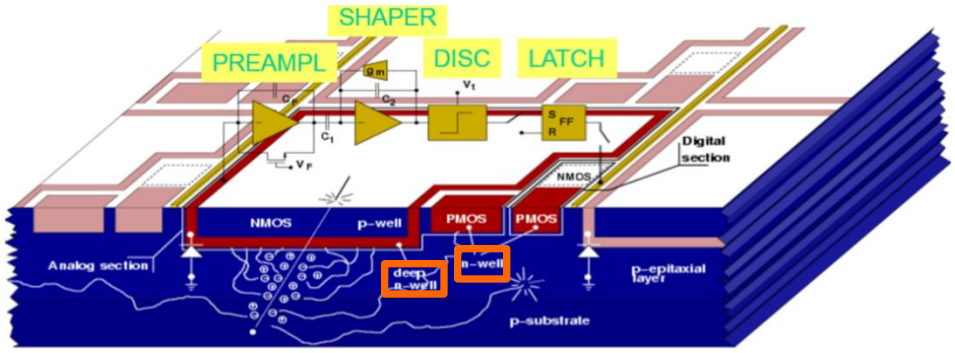
- In-pixel circuitry limited to nMOS transistors only
- pMOS transistors require an n-well implantation
- Any additional n-well (apart from the collecting electrode) collects signal electrons

→ If we include pMOS transistors → loss of sensitivity

MAPS sensors - Technology details



Twin well



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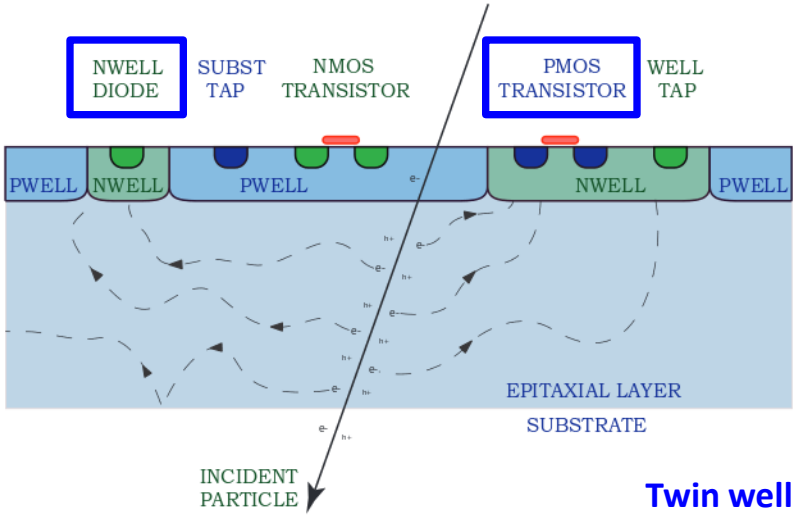
Possible solution 1 (DNW MAPS):

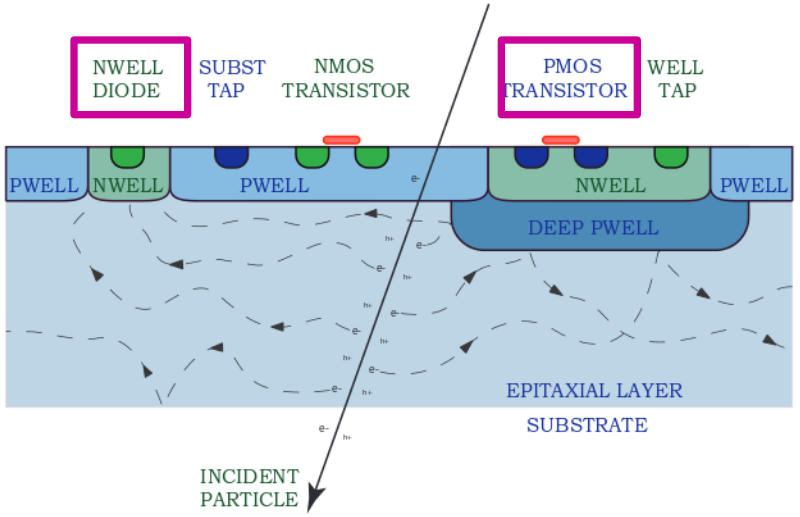
- Use a techno. process with (STMicroelectronics 130 nm):
  - N-well (bulk of pMOS transistors)
  - P-well (bulk of nMOS transistors)
  - **Deep n-well (collecting electrode)**
- **Pixel = sensing diode + fully CMOS amplifier + shaper + comparator** (More complex electronics inside the pixel area are possible)

→ Charge collection efficiency ~92% (APSEL4D chip)

MAPS sensors - Technology details



Twin well



MAPS limitations:

- In-pixel circuitry limited to nMOS transistors only
- pMOS transistors require an n-well implantation
- Any additional n-well (apart from the collecting electrode) collects signal electrons

→ If we include pMOS transistors → loss of sensitivity

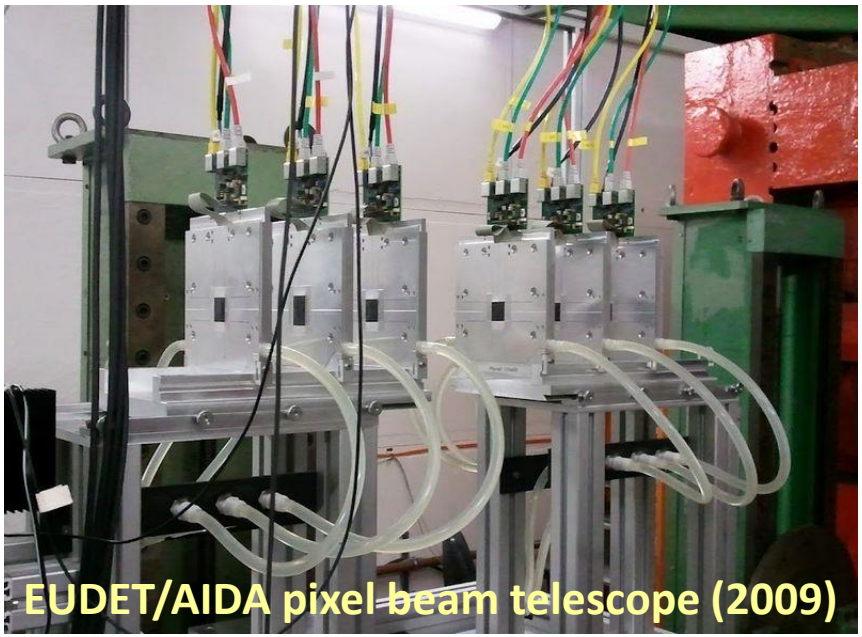
Possible solution 2 (INMAPS):

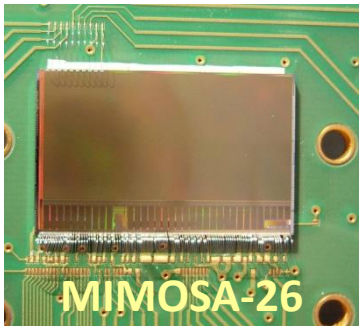
- Use a techno. process with (TowerJazz 180 nm):
  - N-well (collecting electrode)
  - P-well (bulk of nMOS transistors)
  - **Deep p-well (n-well/p-epi isolation)**

- **Pixel = sensing diode + fully CMOS amplifier + shaper + comparator** (More complex electronics inside the pixel area are possible)

→ Charge collection efficiency ~100%

MAPS sensors - HEP applications


EUDET/AIDA pixel beam telescope (2009)

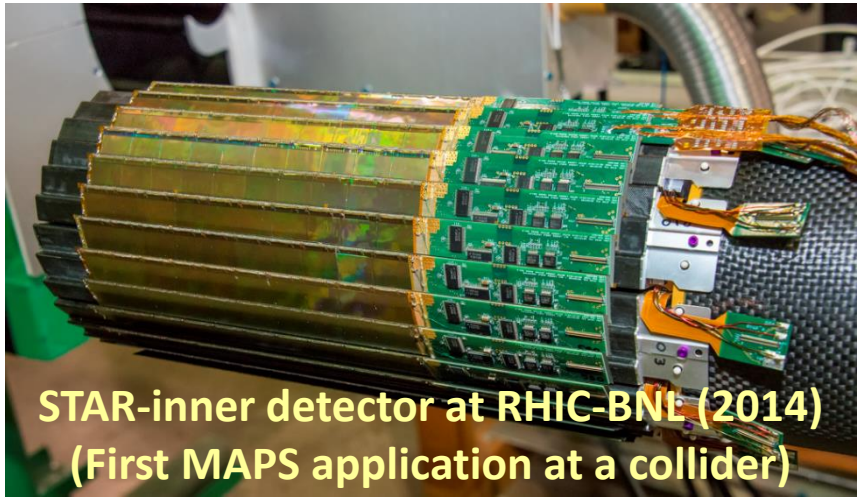

MIMOSA-26

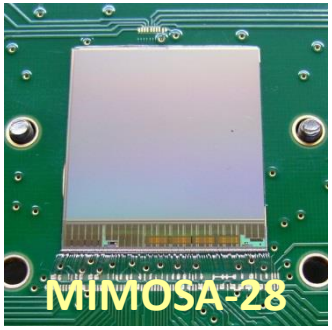
MIMOSA-26

- **Chip size** 13.7 mm x 21.5 mm
- **Sensor matrix** 576 x 1152 pixels (~0.7M pixels)
- **Pixel pitch** 18.4 µm x 18.4 µm
- **Techno. process** AMS 0.35 µm OPTO (twin well)
- **Epitaxial layer** 14 µm
- **Fabrication** 2008

- **Readout electronics:**
  - in-pixel amplification
  - correlated double sampling
  - EOC with discriminator
  - zero suppression
  - on-chip memory to store digital signals
  - readout in a rolling shutter mode (115.2 µs)

MAPS sensors - HEP applications



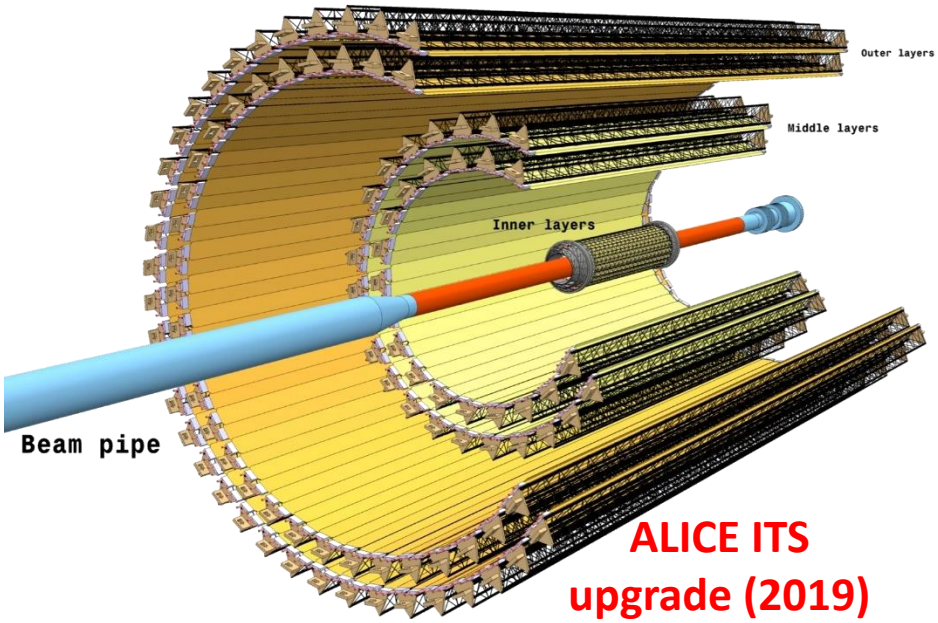


MIMOSA-28 (ULTIMATE)

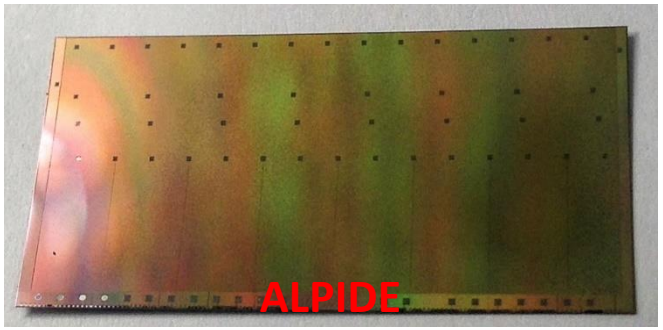
- **Chip size** 20.22 mm x 22.71 mm
- **Sensor matrix** 928 x 960 pixels (~0.9M pixels)
- **Pixel pitch** 20.7 µm x 20.7 µm
- **Techno. process** AMS 0.35 µm OPTO (twin well)
  TID 150 krad
  NIEL few 10^{12} 1 MeV n_{eq}/cm^2
- **Epitaxial layer** 15 µm (>400 Ω·cm)
- **Fabrication** 2011

- **Readout electronics:**
  - in-pixel amplification
  - correlated double sampling
  - EOC with discriminator
  - zero suppression
  - on-chip memory to store digital signals
  - readout mode by rows (185.6 µs)

MAPS sensors - HEP applications



ALICE ITS upgrade (2019)



ALPIDE

- **Chip size** 15 mm x 30 mm
- **Sensor matrix** 512 x 1024 pixels (>0.5M pixels)
- **Pixel pitch** 28 µm x 28 µm
- **Techno. process** TowerJazz 180 nm (quad. well)
  TID 700 krad
  NIEL 10^{13} 1 MeV n_{eq}/cm^2
- **Epitaxial layer** 18-40 µm (>1k Ω·cm)
- **Fabrication** 2014 (CERN, INFN, CCNU, Yonsei)

- **Readout electronics:**
  - in-pixel amplification/discrimination
  - integration time ~4 µs
  - hit recording and pixel address generation
  - data-driven readout (async. priority encoder)
  - readout time α to chip occupancy
    - 1 hit/column (foreseen) → ~10 µs

MAPS sensors - Practical advantages

- Fabricated in **commercial CMOS technologies** → **leading edge performance and low-cost**
- In-pixel amplification
- In-pixel processing electronics are also possible → **very strong signal at pixel output**
- **Readout and digitization electronics can be integrated on the same chip** with the pixel array
- Very small pixel sizes are possible (18 µm x 18 µm) → **high granularity**
- Low leakage current + small sensor capacitance → **excellent noise performance** (~10 e^- per pixel)
- 14-20 µm thick epi layer → **high signal-to-noise ratio** (1 MIP generates ~1000 e^-)
- Epi layer is underneath the readout electronics → **100% fill-factor**
- **Back-thinning to 50 µm is possible** whilst sensor performance is unaffected
- **CMOS sensors have demonstrated excellent performance** (EUDET/AIDA telescope, STAR at RHIC-BNL)

- Why are we developing **HV-CMOS sensors** ??

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- **CMOS sensors have demonstrated excellent performance** (EUDET/AIDA telescope, STAR at RHIC-BNL)
- **Low bias voltage → charge collection by diffusion → long charge collection times (<100 ns)**
- **Limited radiation tolerance → <1 Mrad (TID), <$2 \cdot 10^{13}$ 1 MeV n_{eq}/cm^2 (NIEL)**

- Is that **a problem** ??

  - Let's take a look at **future HEP experiments**

Future HEP experiments - ATLAS ITk upgrade

- **LHC upgrade** → Aimed at determining the Higgs boson properties and looking for new physics
  - Higher centre-of-mass energy and luminosity:

Upgrade	Year	√s (TeV)	L ($cm^{-2}s^{-1}$)	BX-time (ns)	intL (fb^{-1})
LHC Phase 0	2015	13~14	~$1 \cdot 10^{34}$	25	~75-100
LHC Phase I	2018	14	~$2 \cdot 10^{34}$	25	~350
HL-LHC Phase II	>2025	14	$5 \cdot 10^{34}$	25	~3000

  - Major challenges:
    - Higher data rates → improved TDAQ
    - Higher occupancy → finer granularity
    - More radiation damage → more rad-hard sensors and electronics

HL-LHC Phase II	TID (MRad)	NIEL (1 MeV n_{eq}/cm^2)
Inner detector	>1000 (*)	$2 \cdot 10^{16}$ (*)

(*) including a safety 2 factor

  - To operate in such a harsh environment, **a major detector upgrade is necessary**
  - Idea → explore **industry standard processes as replacement sensors** (low-cost)

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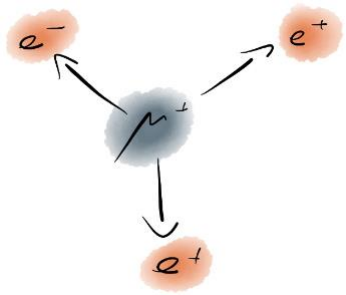
  - To operate in such a harsh environment, **a major detector upgrade is necessary**
  - Idea → explore **industry standard processes as replacement sensors** (low-cost)
    - **MAPS sensors offer many advantages, but they are not suited for the ATLAS ITk upgrade**

Future HEP experiments - Mu3e experiment



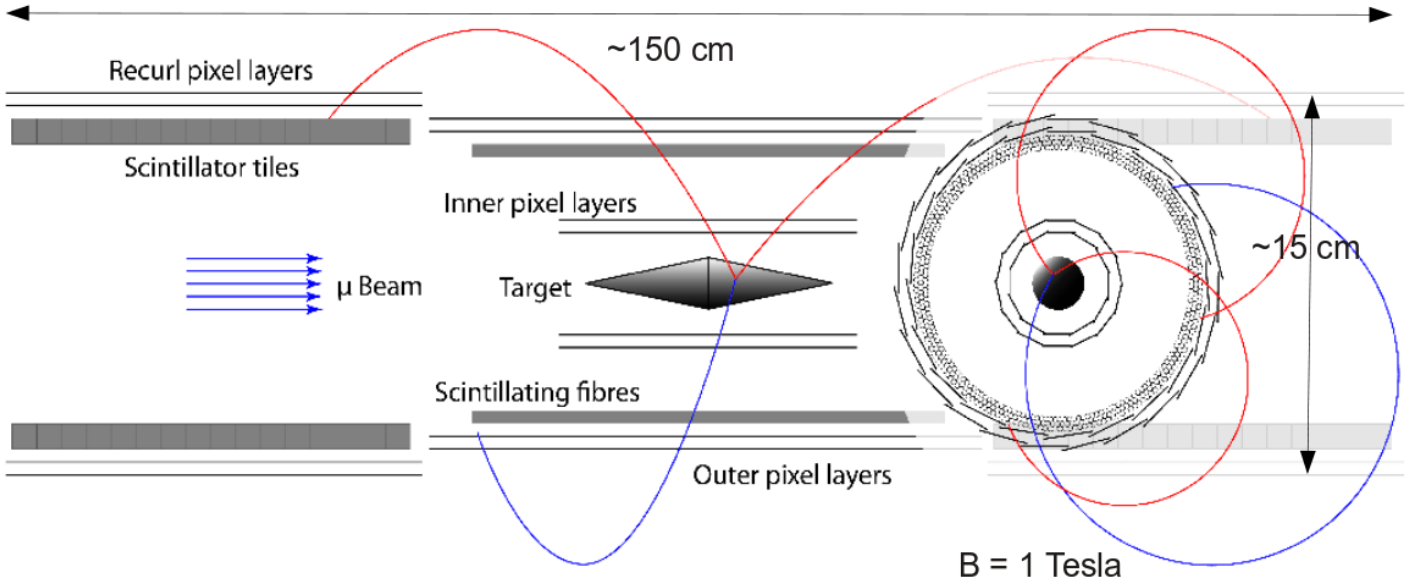
- **Target** → Search for new physics beyond the Standard Model
  - By looking at the lepton flavor violating decay $\mu^+ \rightarrow e^+e^-e^+$
- **Challenges**
  - Extreme BR sensitivity (10^{-15} Phase I, 10^{-16} Phase II) → continuous high current beam of $>10^8$ (PI)-10^9 (PII) muons/s (PSI) → detector capable of coping with this rate
  - Reduce backgrounds ($>10^{-15}$ Phase I, $>10^{-16}$ Phase II) → excellent momentum & time measurement of low-energy electrons (<53 MeV/c)
- **These requirements drive the detector design:**

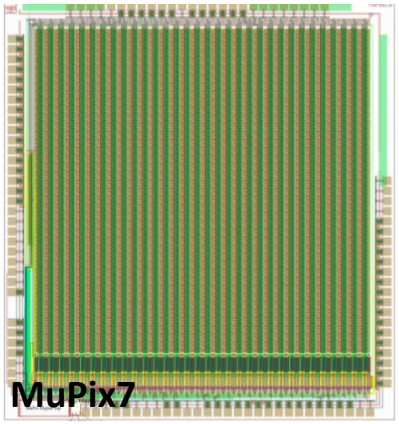
Pixel size	Time resolution	Material budget	Efficiency
80 μm x 80 μm	<20 ns (PI) <1 ns (PII)	~0.1% X_0 per layer (detector 50 μm)	>99%

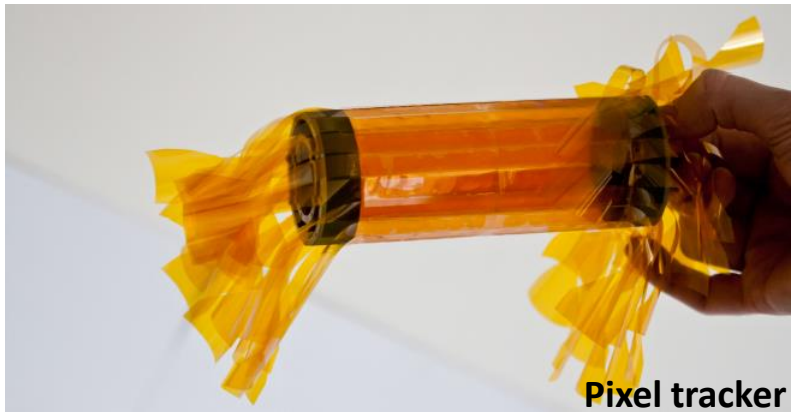
Phase I → 2017
Phase II → >2020

- Other requirements in terms of low power consumption (<150 mW/cm^2)
- **Mu3e is the first experiment that will see HV-MAPS (MuPix) operate in a real application!**

Future HEP experiments - Mu3e experiment




MuPix7


Pixel tracker

Future HEP experiments - ILC and CLIC

- **ILC and CLIC** → Two proposed linear e^+-e^- colliders to study the Higgs boson properties in great detail

Collider details:

Beam parameter	ILC	CLIC
E (TeV)	1	3
L ($cm^{-2}s^{-1}$)	$2.70 \cdot 10^{34}$	$5.90 \cdot 10^{34}$
BX-time (ns)	337	0.5
#Bunches/train	2820	312
Inter-train (ms)	199	~20
#Particles/bunch	$7.50 \cdot 10^{9}$	$3.72 \cdot 10^{9}$
σ_x/σ_y (nm/nm)	640/5.7	40/1

In an ILC/CLIC environment, MAPS could work well with 50 µs time-slicing and 25 µm x 25 µm pixel size

Requirements on tracking detectors:

Detector requirement	Value
σ_{point}	<5 µm (pixel pitch of 17 µm)
Material budget/layer	<0.15% X_0 (ILD) <0.30% X_0 (SiD)
Granularity	High
Occupancy	<1%
Radiation tolerance	100 krad/year (TID, ILC) 10^{11} 1 MeV n_{eq}/cm^2/year (NIEL, ILC) 20 krad/year (TID, CLIC) $4 \cdot 10^{10}$ 1 MeV n_{eq}/cm^2/year (NIEL, CLIC)
Power	<a few mW/cm^2
Cost	Low

HV-CMOS sensors

- **MAPS** are excellent sensors with many practical advantages, but **charge collection via diffusion** makes them

  - too slow
  - not sufficiently radiation tolerant

  for certain experiments.

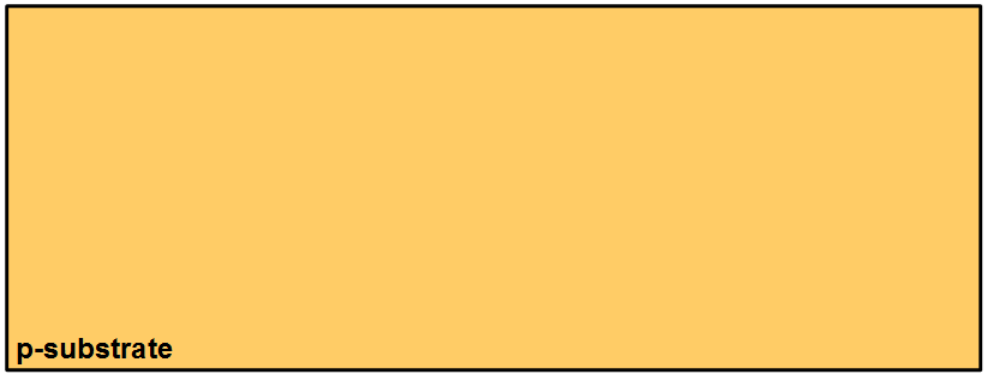
- **High Voltage-MAPS (HV-MAPS)** combine the advantages of MAPS with a “high” voltage of up to 120 V which is applied between the substrate and deep n-wells containing the transistors. This voltage leads to

  - fast charge collection via drift
  - better radiation tolerances.

- How can we **implement an HV-CMOS sensor** ??

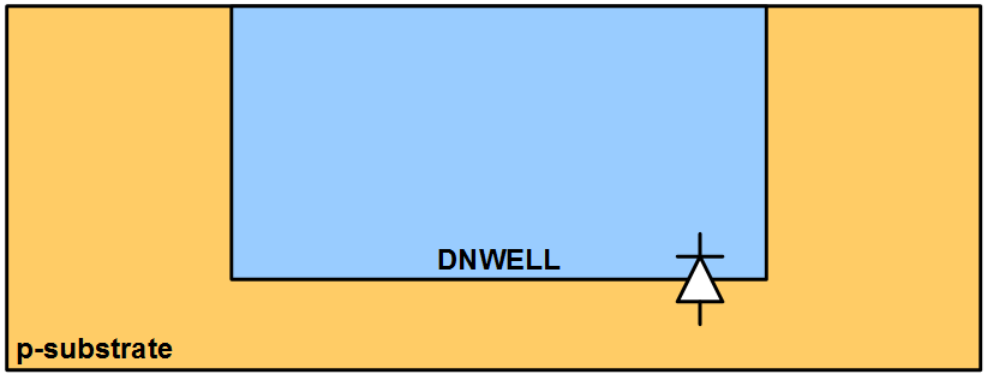
HV-CMOS sensors - Technology details

- The majority of commercial HV-CMOS technologies use p-type substrates



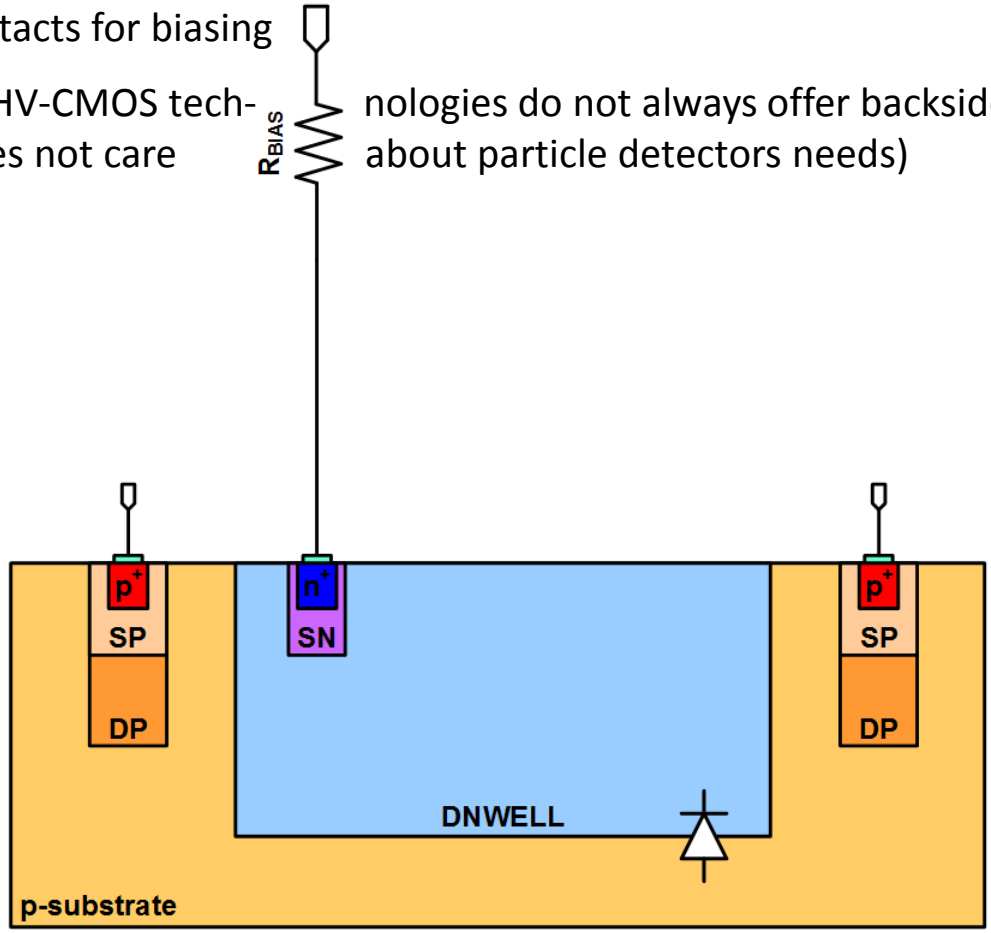
HV-CMOS sensors - Technology details

- A DNWELL/p-substrate diode is the sensing element



HV-CMOS sensors - Technology details

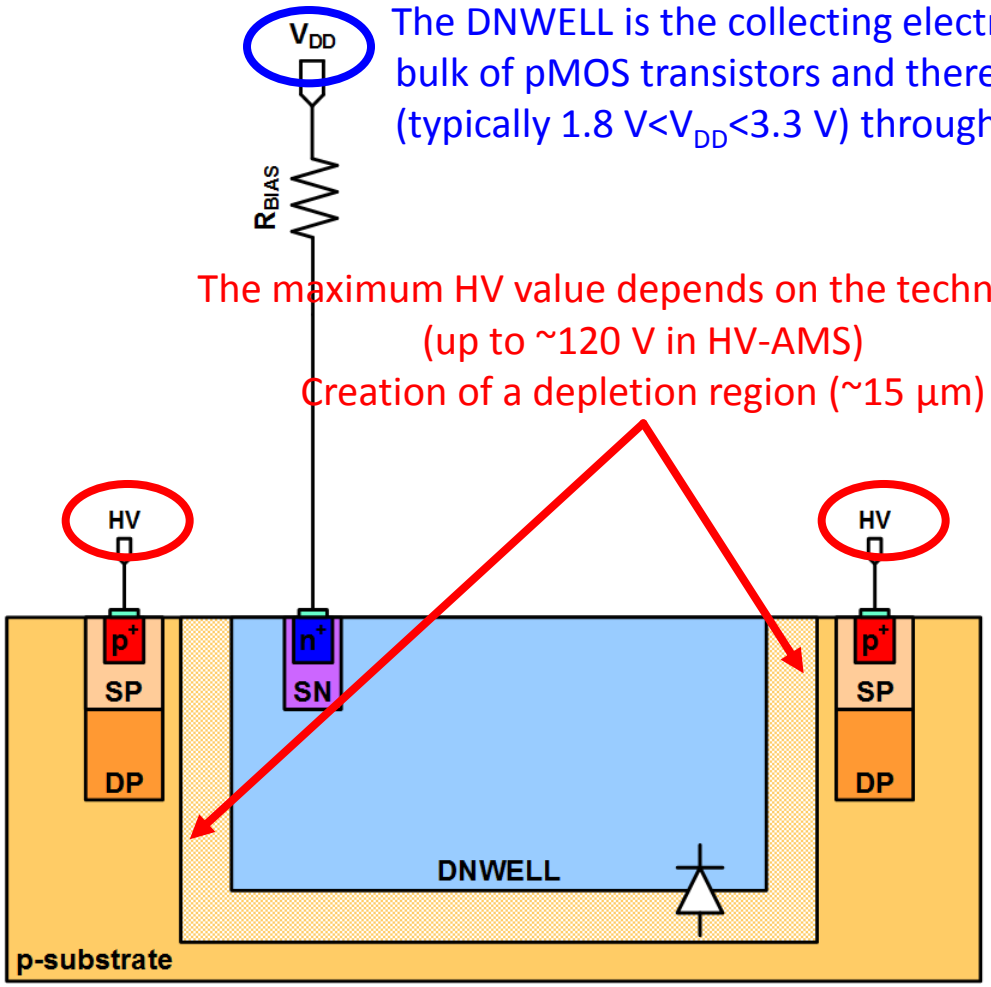
- We need contacts for biasing
- Commercial HV-CMOS tech- nologies do not always offer backside processing (industry does not care about particle detectors needs)



HV-CMOS sensors - Technology details

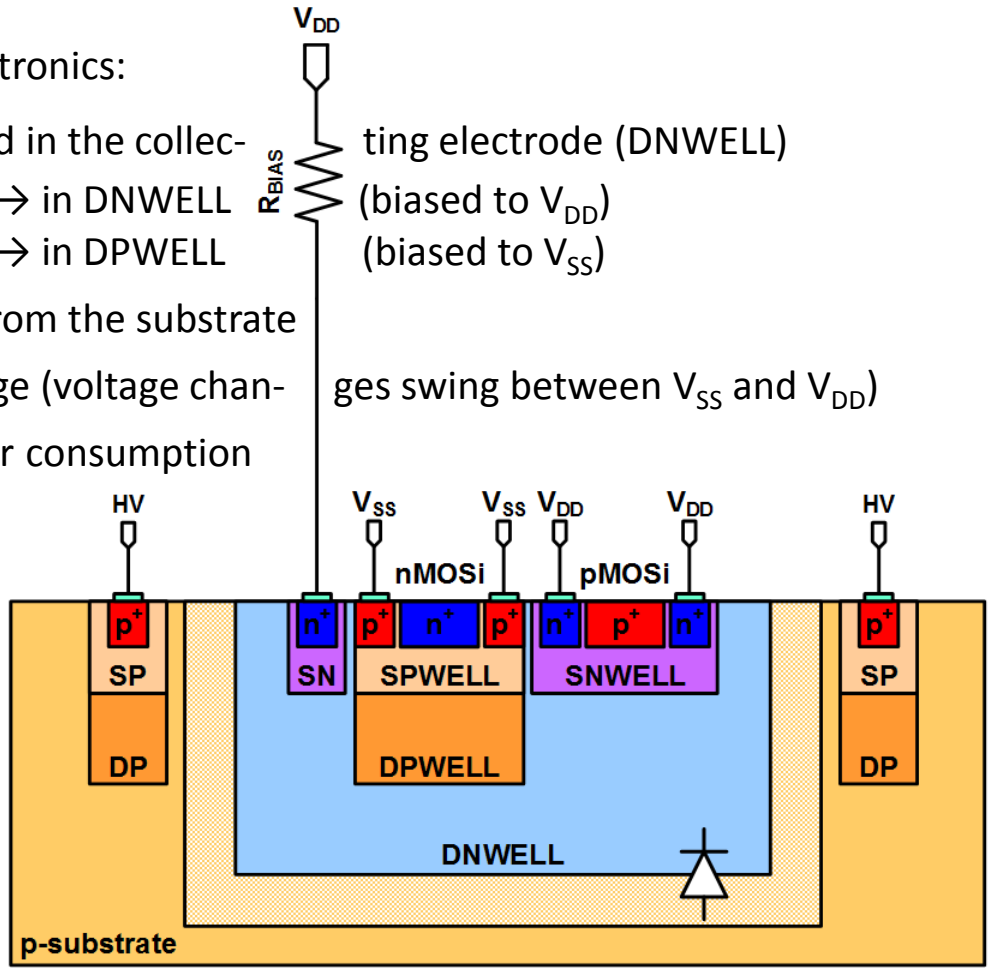
The DNWELL is the collecting electrode, but also the bulk of pMOS transistors and therefore biased to V_{DD} (typically 1.8 V<V_{DD}<3.3 V) through a resistor

The maximum HV value depends on the technology
(up to ~120 V in HV-AMS)
Creation of a depletion region (~15 µm)



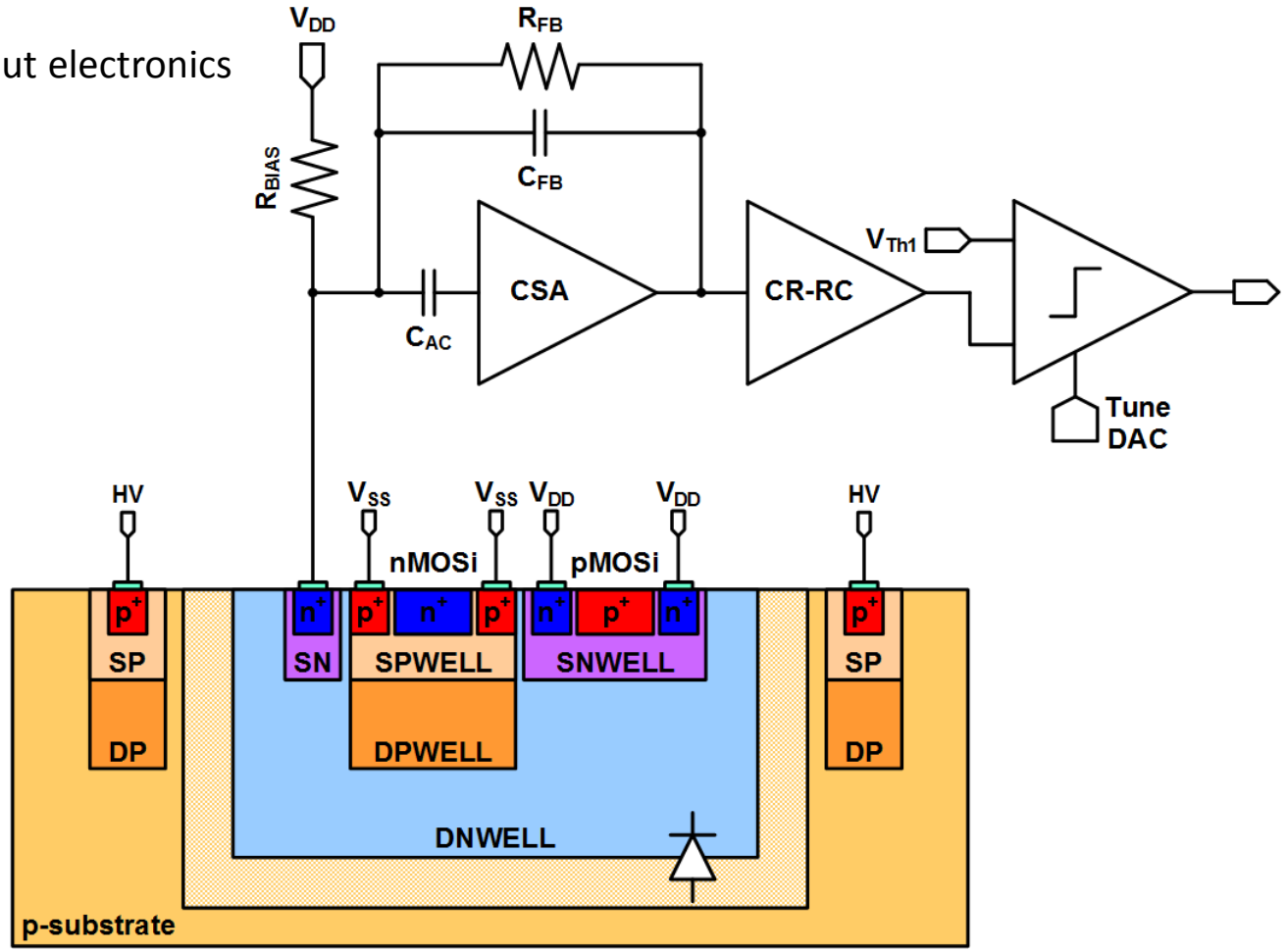
HV-CMOS sensors - Technology details

- Readout electronics:
  - embedded in the collecting electrode (DNWELL)
    - pMOS → in DNWELL (biased to V_{DD})
    - nMOS → in DPWELL (biased to V_{SS})
  - isolated from the substrate
  - low-voltage (voltage changes swing between V_{SS} and V_{DD})
  - low-power consumption



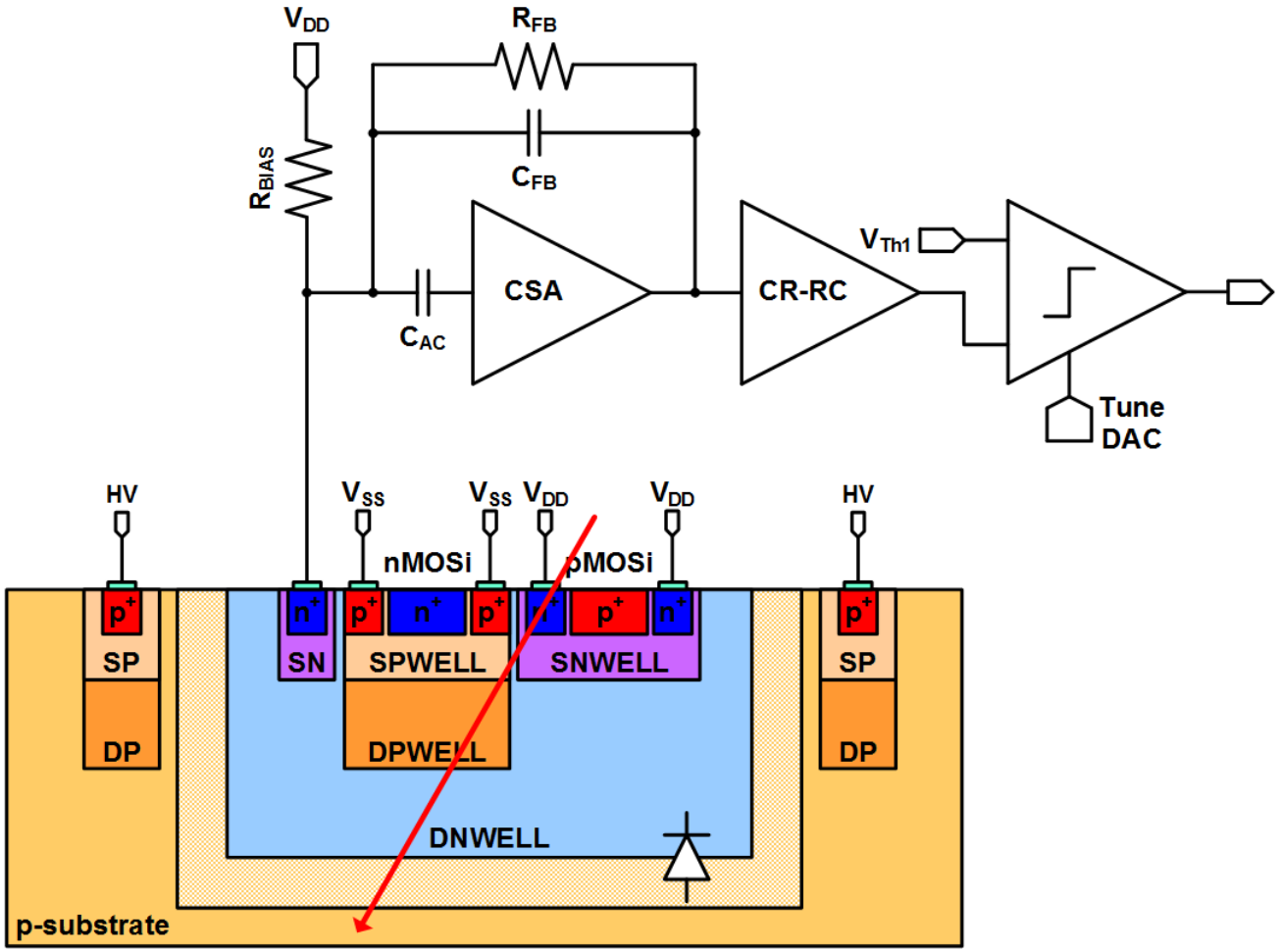
HV-CMOS sensors - Technology details

- Typical readout electronics



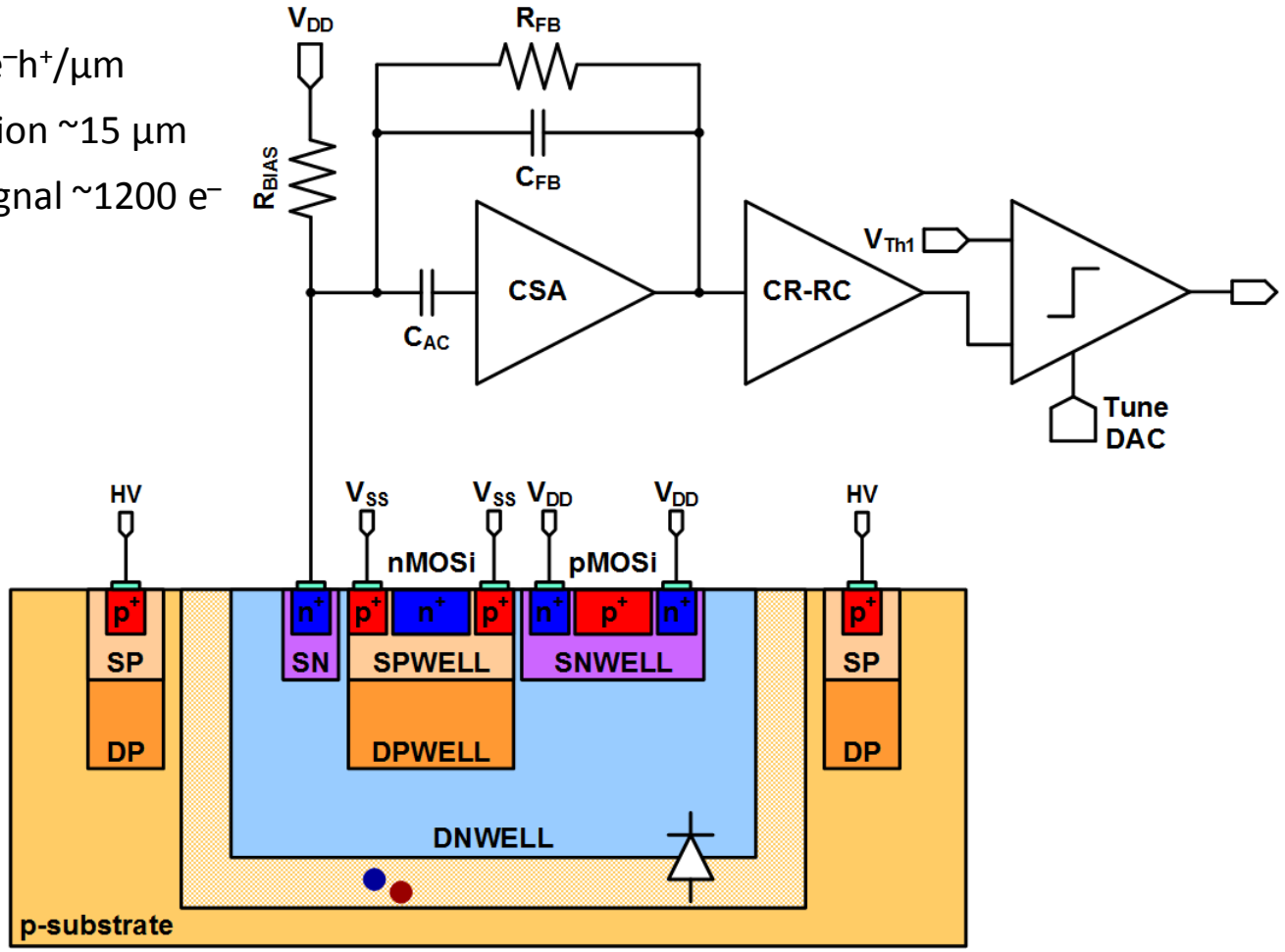
HV-CMOS sensors - Technology details

- 1 MIP



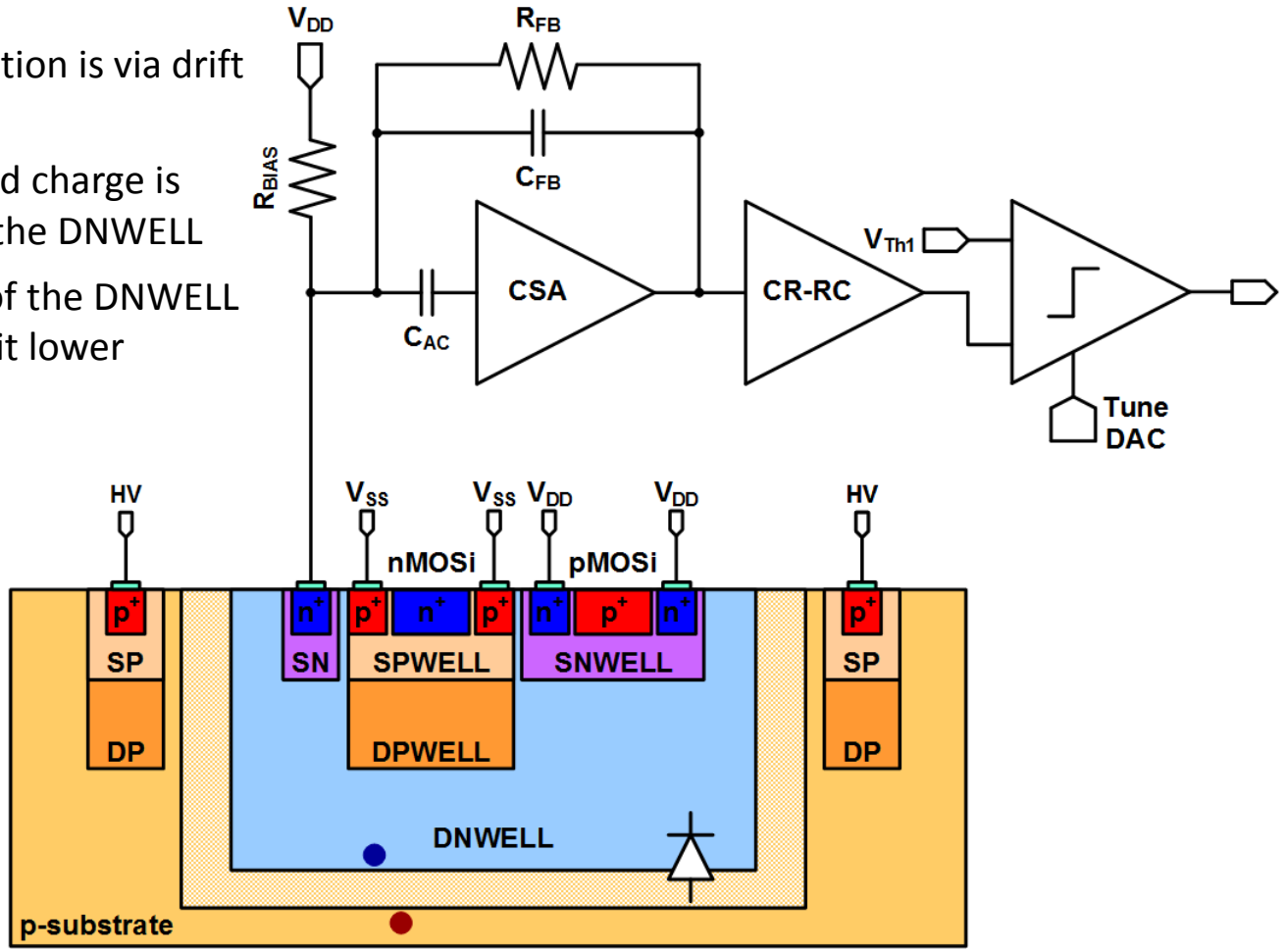
HV-CMOS sensors - Technology details

- 1 MIP → 80 $e^{-}h^{+}/\mu m$
- Depleted region ~15 µm
- Generated signal ~1200 e^{-}



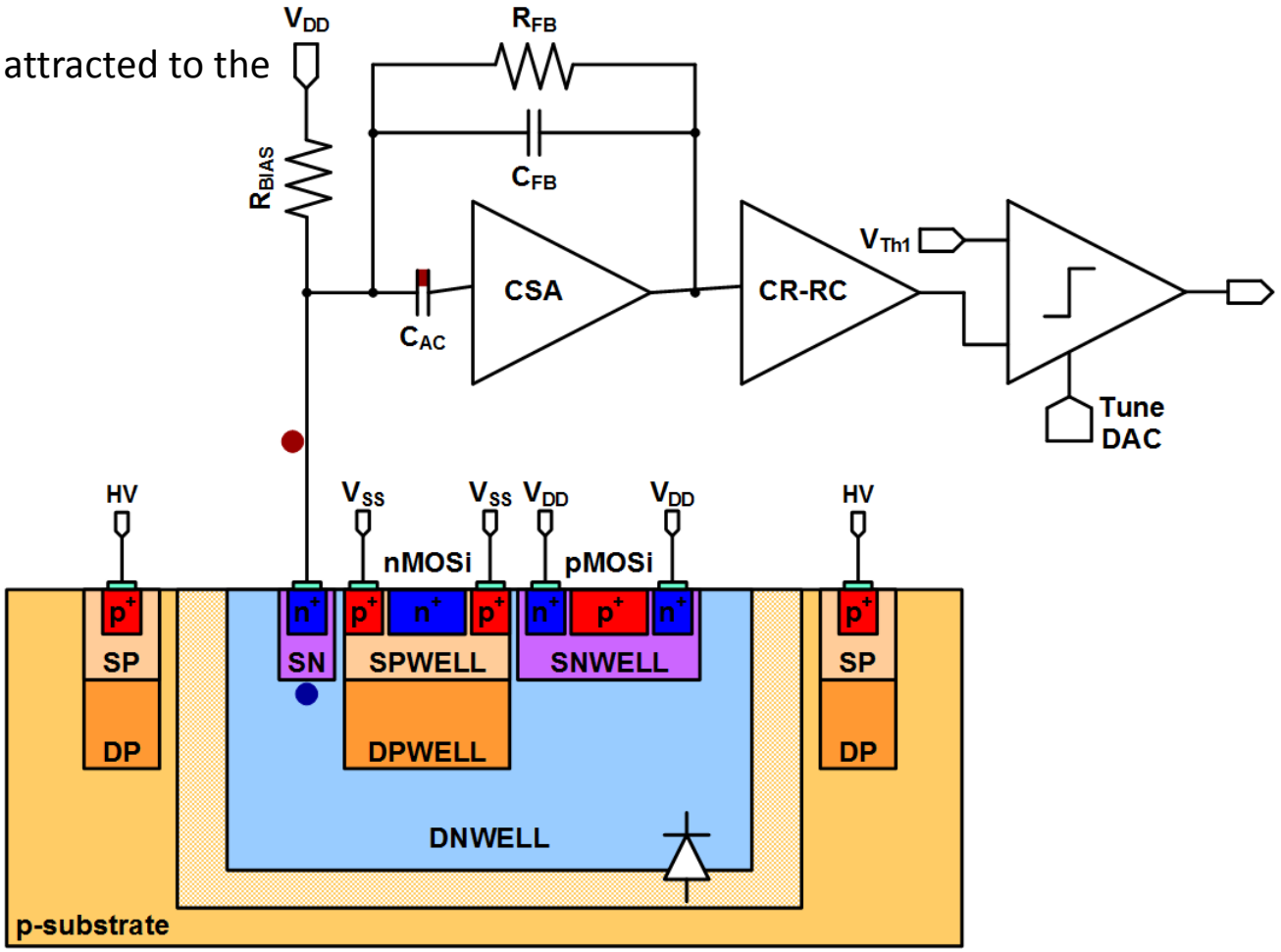
HV-CMOS sensors - Technology details

- Charge collection is via drift (fast, <1 ns)
- The generated charge is collected by the DNWELL
- The voltage of the DNWELL becomes a bit lower



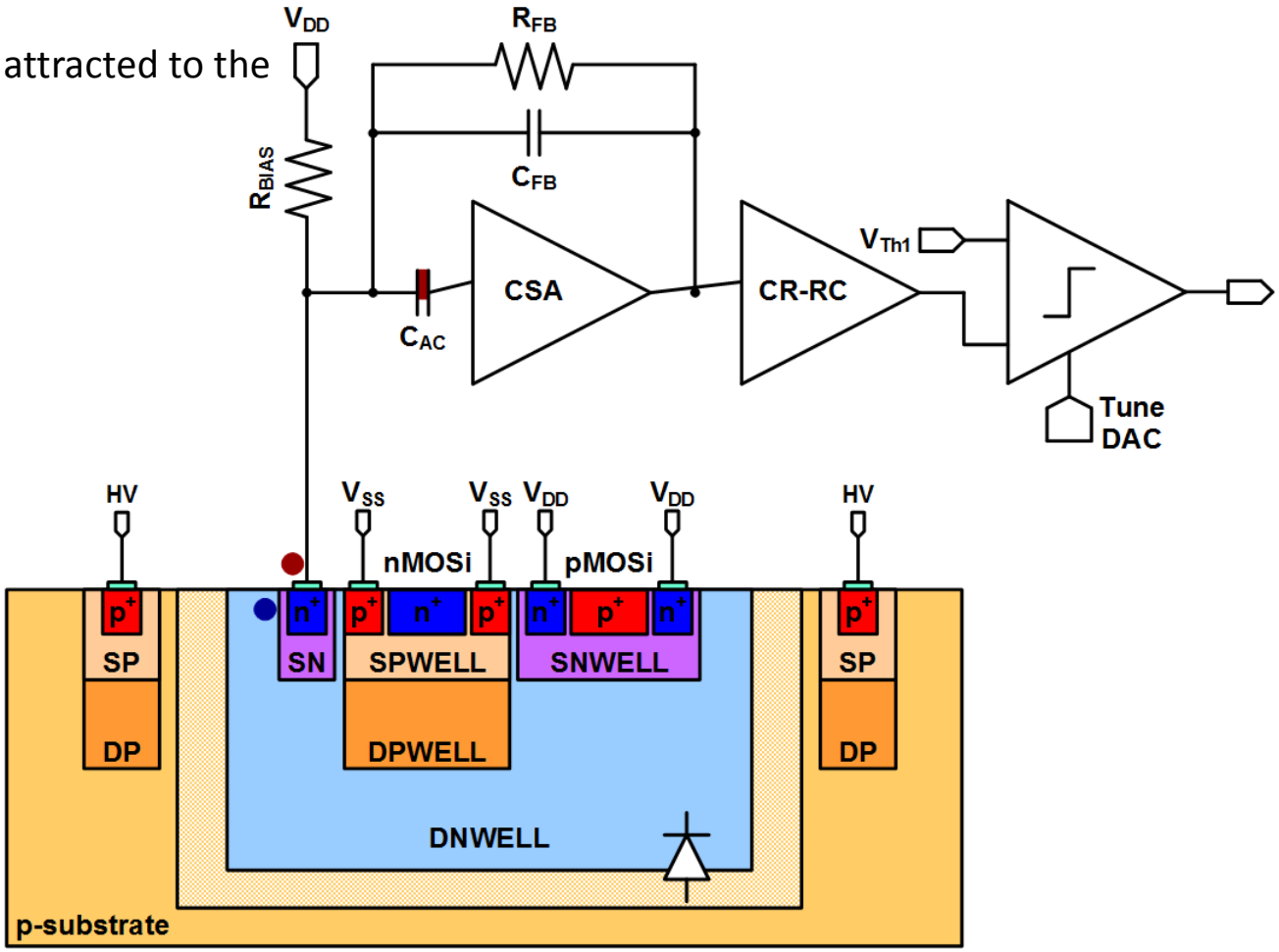
HV-CMOS sensors - Technology details

- The charge is attracted to the contact



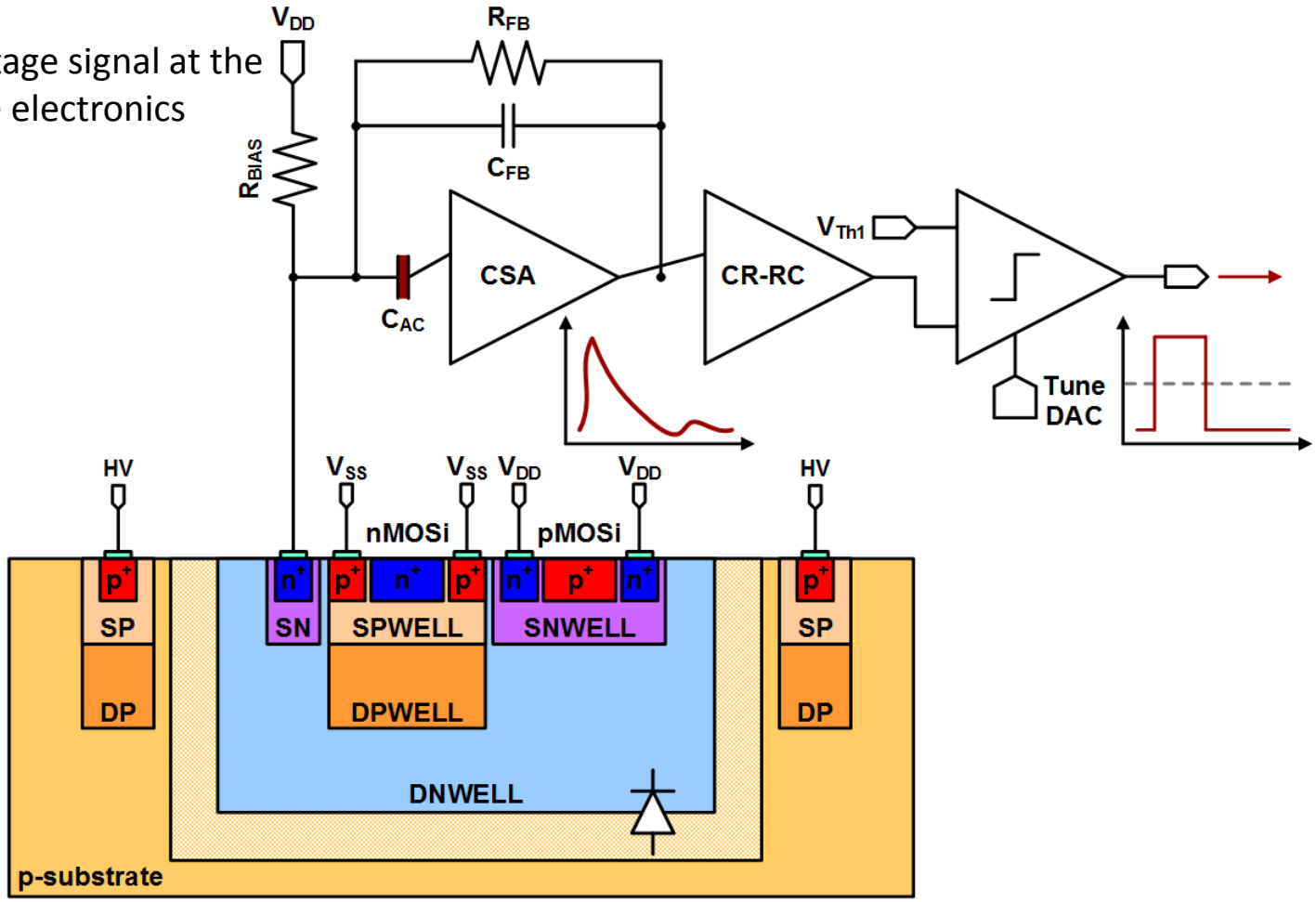
HV-CMOS sensors - Technology details

- The charge is attracted to the contact



HV-CMOS sensors - Technology details

- We see a voltage signal at the output of the electronics



Available foundries

	AMS	LFoundry	ESPROS	XFAB	TowerJazz
Feature node	180 nm/ 0.35 µm	150 nm	150 nm	180 nm	180 nm
HV	≤ 100 V/ ≤ 150 V	≤ 60 V	≤ 15 V	≤ 200 V	≤ 5 V
HR	2016/Yes	Yes	Yes	Yes	Yes
Quadruple well	No (triple)	Yes	Yes	No (BOX)	Yes
Metal layers	6/4	6	6	6	6
Backside processing	No	Yes	Yes	No	Yes
Stitching	No	Yes	No	No	Yes
TSV	Yes	No	No	No	No

- Other options are:
  - Global Foundries 130 nm, IBM 130 nm, OKI/LAPIS/KEK, ON Semiconductor 180 nm (formerly AMIS), Toshiba 130 nm, TSMC 65 nm

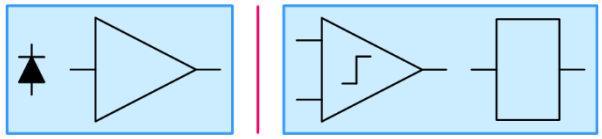
HV-CMOS developments

- **The beginnings:**
  - First chip submitted **in HV-AMS 0.35 µm 2006 by Ivan Peric → proof-of-concept**
    - **to investigate** the properties of the DNWELL/p-substrate diode
    - **to demonstrate** that it is possible to implement complex CMOS electronics in the collecting DNWELL electrode
    - electronics → CSA, CR-RC shaper, discriminator with 4-bit tune DAC, latch and bus driver
    - full functionality of the detector!
    - noise ~80 e^-
- Since then, **many developments under way**:
  - in a **few different technologies** (mostly in HV-AMS 0.35 µm/180 nm and LFoundry 150 nm, but also in ESPROS 150 nm, XFAB 180 nm, TJ 180 nm and others)
  - **aiming at various applications** (ATLAS upgrade, Mu3e and ILC/CLIC)
  - **and by several groups** (CERN, IFAE, KIT, SLAC, Uni. Bonn and Uni. Liverpool).

→ Let's take a look at them! Just a selection.

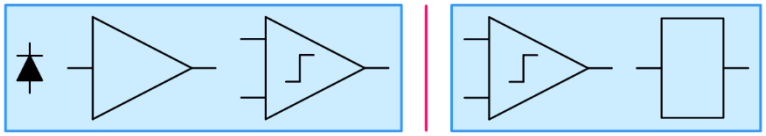
HV-CMOS developments

- **CCPD chips family**
  - **- CCPD = Capacitive Coupled Pixel Detector**
  - - Concept → a detector with large area pixels that can be read out via FE-I4
  - **- Options:**
    - **- HV/HR-CMOS sensor with analogue output + FE-I4 readout (typical option)**
      - - HR/HV-CMOS sensor with CSA



Diode + CSA **FE-I4**

    - **- HV/HR-CMOS sensor with digital output + FE-I4 readout**
      - - HR/HV-CMOS sensor with CSA and discriminator



Diode + CSA + discrimin. **FE-I4**

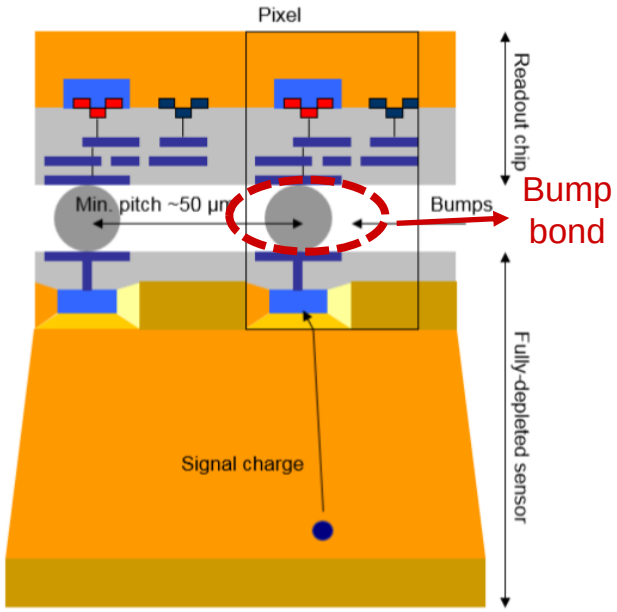
    - **- HV-CMOS/FE-I4 connection via gluing (instead of via bump-bonding)**
    - - **Pixel area** → the same as in FE-I4 (1-to-1 connection)
      smaller than in FE-I4 (**with sub-pixel encoding**, HV2FEI4)

Other options, such as HV/HR-CMOS passive sensor + FE-I4 or readout with other FE chips, are also possible

HV-CMOS developments

- **Traditional sensor/FE-I4 connection (hybrid)**

Via bump-bonding:

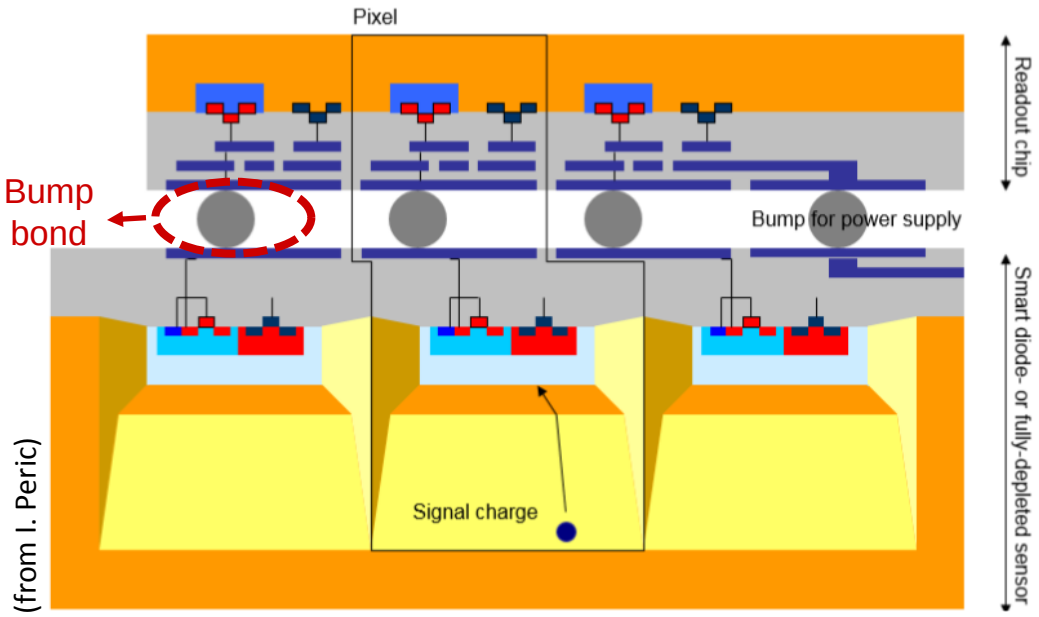


(from I. Peric)

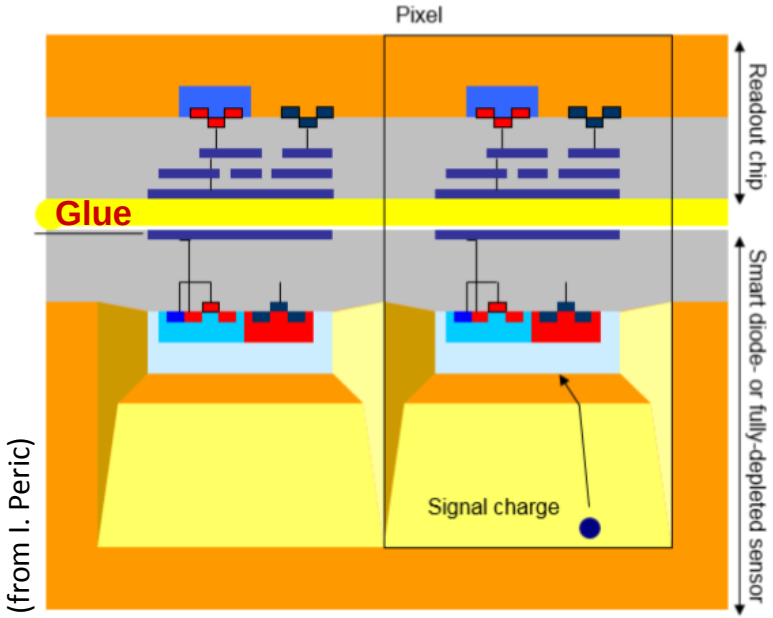
HV-CMOS developments

- **HV-CMOS/FE-I4 connection**

Via bump-bonding:



Via gluing:

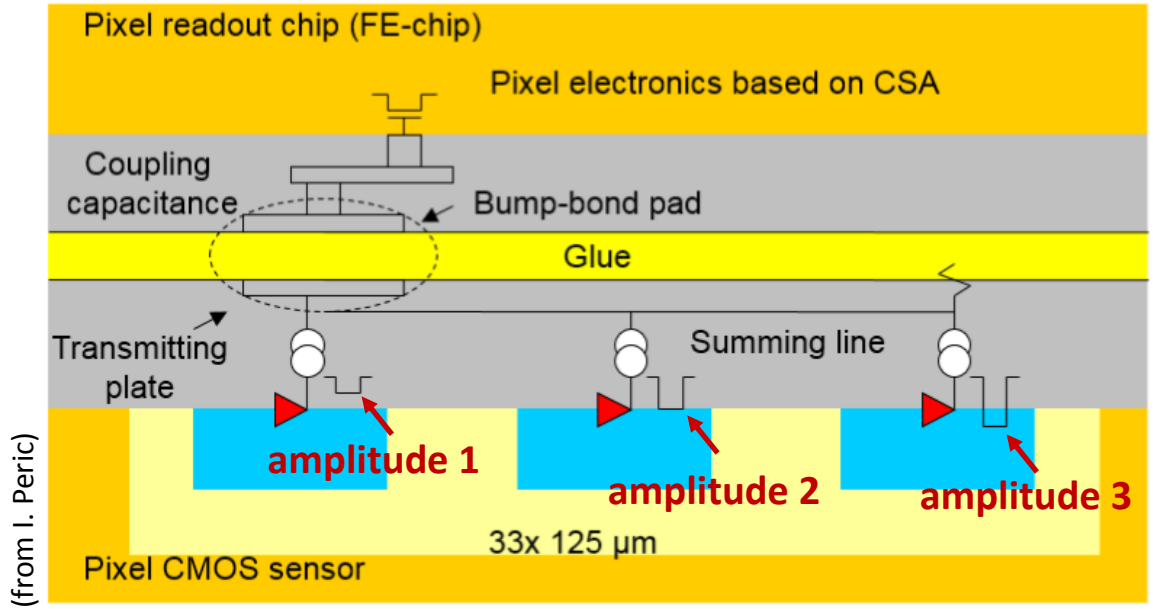


- Lower price
- Better mechanical stability
- Less material

HV-CMOS developments

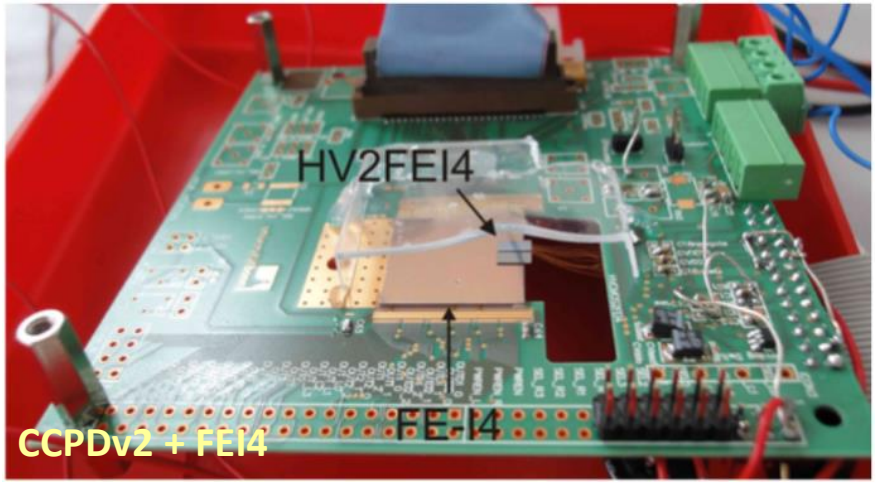
- **Sub-pixel encoding** → Each pixel that is coupled to the same FE-I4 readout cell has a **unique signal amplitude** or **unique signal duration**.

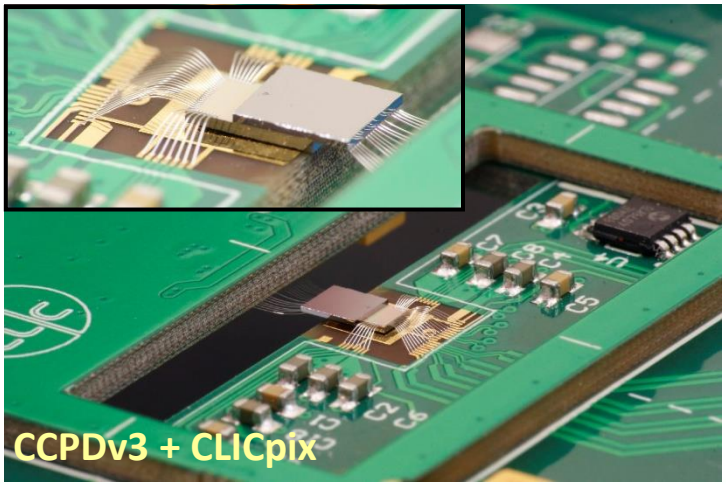
  → The pixel can be identified by examining the amplitude/duration information generated in the FE chip.



HV-CMOS developments

- **CCPD chips family in HV-AMS 180 nm:**
  - CCPDv1 (Nov. 2011) → SNR after $2 \cdot 10^{15}$ n_{eq}/cm^2 (neutrino irradiation) ~20. Test-beam.
  - CCPDv2 (Nov. 2012) → works after 862 Mrad (X-ray irradiation). Test-beam.
    efficiency before irradiation is >99% and after irradiation ~95%.
  - CCPDv3 (Nov. 2013) → pixels match the CLICPix 65nm ASIC developed for CLIC
  - CCPDv4 (Jun. 2014)
  - CCPDv5 (Feb. 2015) → improved version of CCPDv4
    improved guard ring structure that allows for higher HV (<120 V)
    time-walking compensation in-pixel

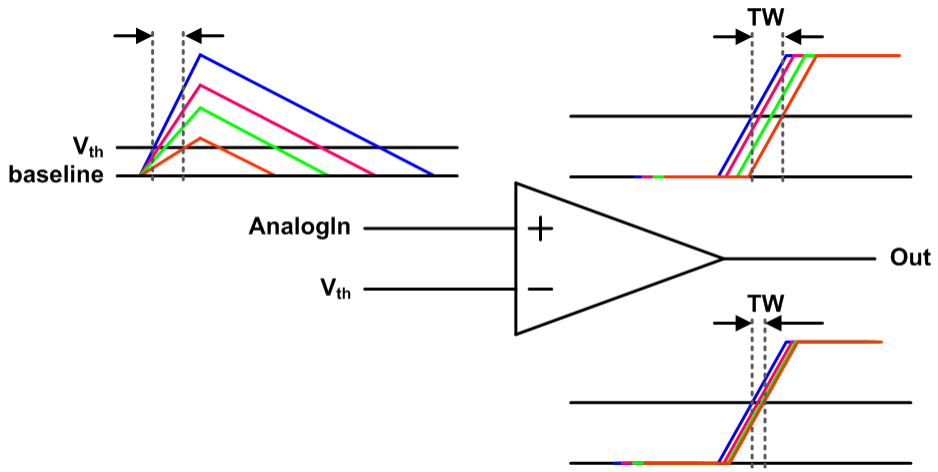




HV-CMOS developments

- **Discriminator:**

- Low and high energy particles generate signals that cross the threshold voltage at different times (also the response time of the electronics is dependent on the signal strength). This time difference is the time walk.
- Idea of time walk compensation → The propagation time through the comparator is independent of the amplitude of the signal generated by the sensor.

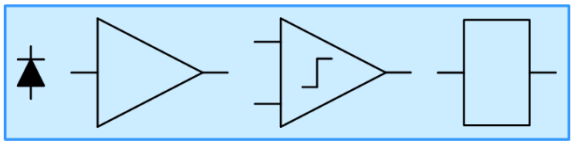


Without compensation
(TW ≈ 25 ns with
standard resistivity)

With compensation
(TW ≈ a few ns only)

HV-CMOS developments

- **MuPix chips family in HV-AMS 180 nm:**
  - MuPix chips are fully monolithic pixel detectors



Diode + CSA + discrimin. + digital readout

  - The digital readout cell is placed at the periphery of the sensing matrix:
    - Time-stamp generation upon particle hit
    - Time-stamp and pixel address are stored in on-chip memories until readout
    - Priority logic controls the readout order (~99% efficiency measured in test beams)
  - More complex electronics integrated at each new MuPix generation:

Prototype	In-pixel CSA	2nd amplifier	Comparator	Serial Gigabit link	Internal state machine
MuPix4	✓		Standard		
MuPix6	✓	✓	New		
MuPix7	✓	✓	New	✓	✓

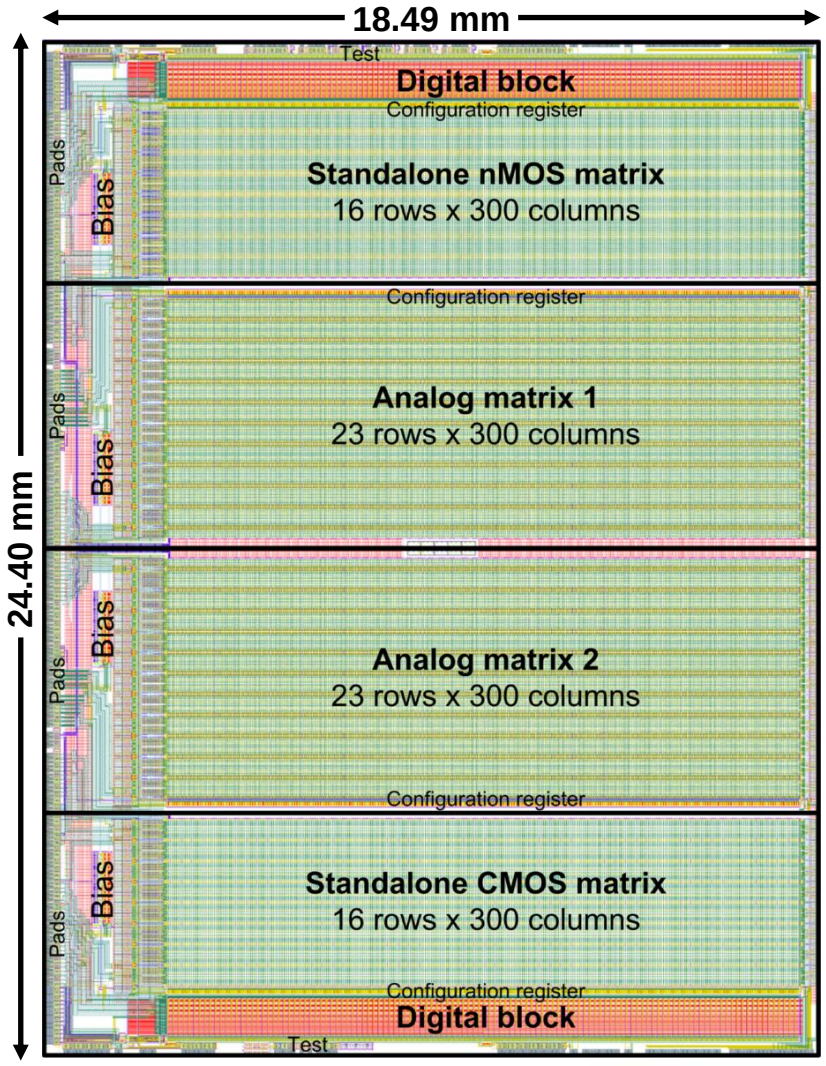
  - Currently working towards **MuPix8**, **a large area chip (HR) that will be submitted in 2016**

HV-CMOS/HV-MAPS sensors - Main properties

- In industry standard HV-CMOS technologies **(mature, low-cost)**
- High negative bias voltage for a **wide depletion region** (15 µm) in the substrate
  - **Fast charge collection** (~200 ps)
  - **High radiation tolerance** (~10^{15} n_{eq}/cm^2, ~1 GRad)
- **Small pixels** (~25 µm x 25 µm)
- **Thin sensors** (≥50 µm)
- **High integration density of CMOS electronics**
  - Embedded in the collecting electrode
  - Isolated from the substrate
- **Compatibility with existing readout ASICs** (FE-I4)
- **Possibility of digital readout electronics** in the sensor layer (HV-MAPS or smart sensors)
  - Generation of time-stamps and pixel addresses
- Possibility of using **substrates with higher resistivities to widen the depletion region**
  - Less detector capacitance (less noise) and more signal amplitude
- Excellent detection efficiency (>95%) and position resolution (~3 µm), good time resolution (<20 ns)

- The University of Liverpool started in 2014 an **R&D programme to develop HV-CMOS sensors**

H35DEMO - Main features



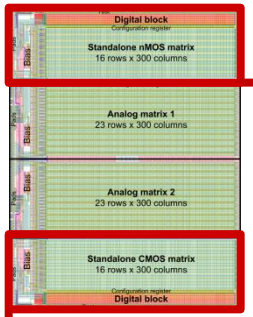
Main features:

- ams 0.35 µm High-Voltage CMOS (H35)
- submission through an engineering run
  - submission in October 2015
  - wafer production finished in December 2015
- different substrate resistivities to improve SNR
  - 20 Ω·cm (standard), 80 Ω·cm, 200 Ω·cm, 1k Ω·cm

Areas (from top to bottom):

- standalone nMOS matrix
  - digital pixels with in-pixel nMOS comparator
  - standalone readout
- analog matrix (2 identical arrays)
  - different flavours in terms of gain and speed
- standalone CMOS matrix
  - analog pixels with off-pixel CMOS comparator
  - standalone readout

H35DEMO - Design aspects



nMOS comparator:

- 150 columns with simple comprator
- 150 columns with TW compensated comparator

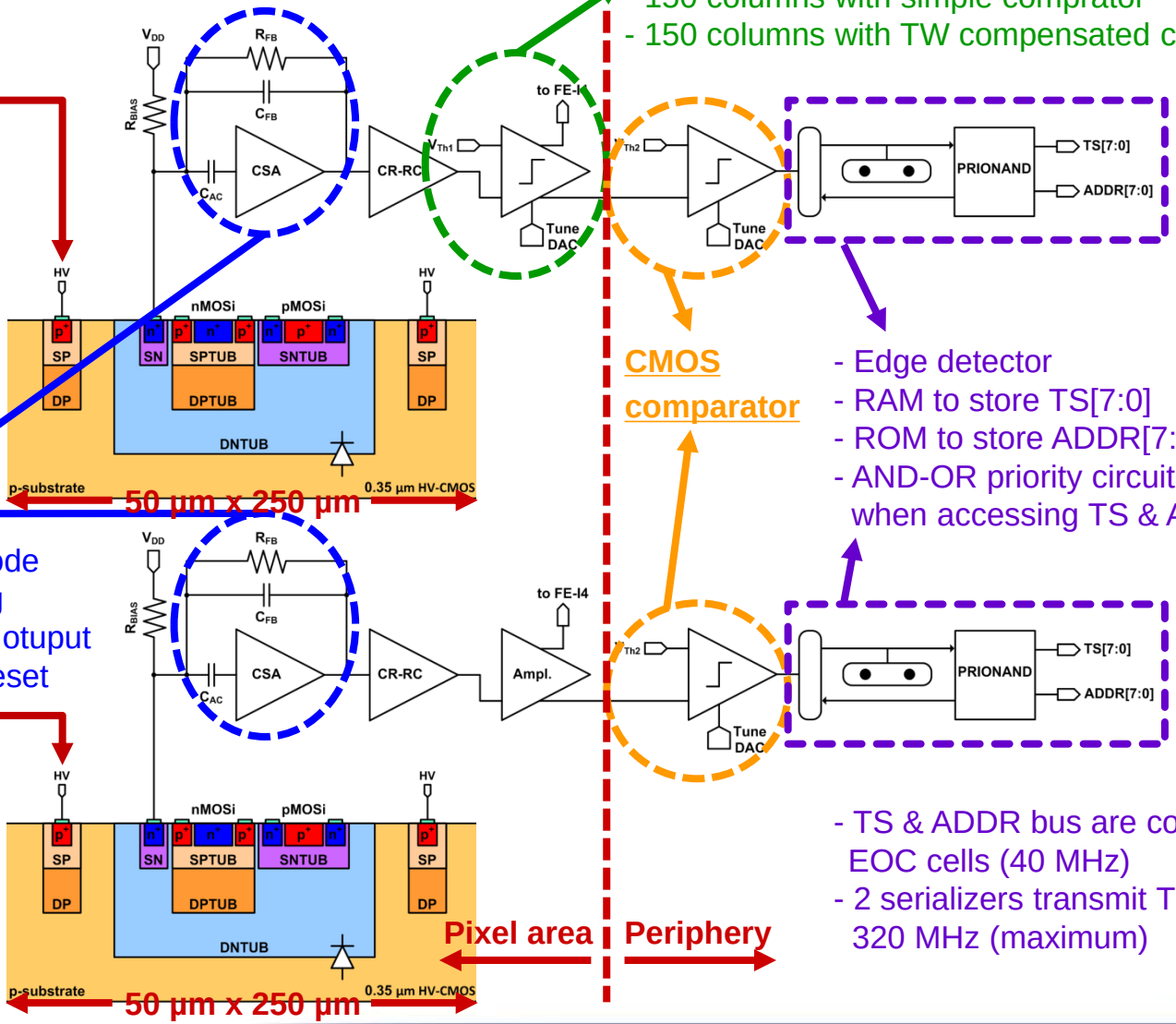
CSA:

- Folded Cascode
- Gain boosting
- Single ended otuput
- Continuous reset

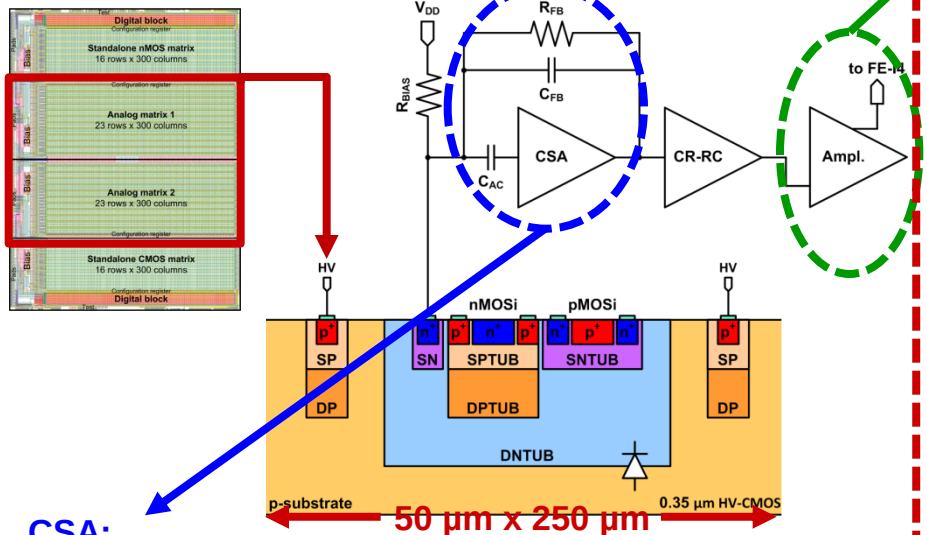
CMOS comparator

- Edge detector
- RAM to store TS[7:0]
- ROM to store ADDR[7:0]
- AND-OR priority circuit to avoid conflics when accessing TS & ADDR bus

- TS & ADDR bus are connected to EOC cells (40 MHz)
- 2 serializers transmit TS & ADDR at 320 MHz (maximum)



H35DEMO - Design aspects



CSA:

- Folded Cascode
- Gain boosting
- Single ended otuput
- Continuous reset

2nd amplifier

1st analog matrix:

- CSA uses nMOS as input transistor
  → less noise, better radiation tolerance
  → more power consumption
- CSA without gain boosting
- First 100 columns with extra HV
- First 200 columns with ELTs in FB block
- Last 100 columns with linear transistors in FB block

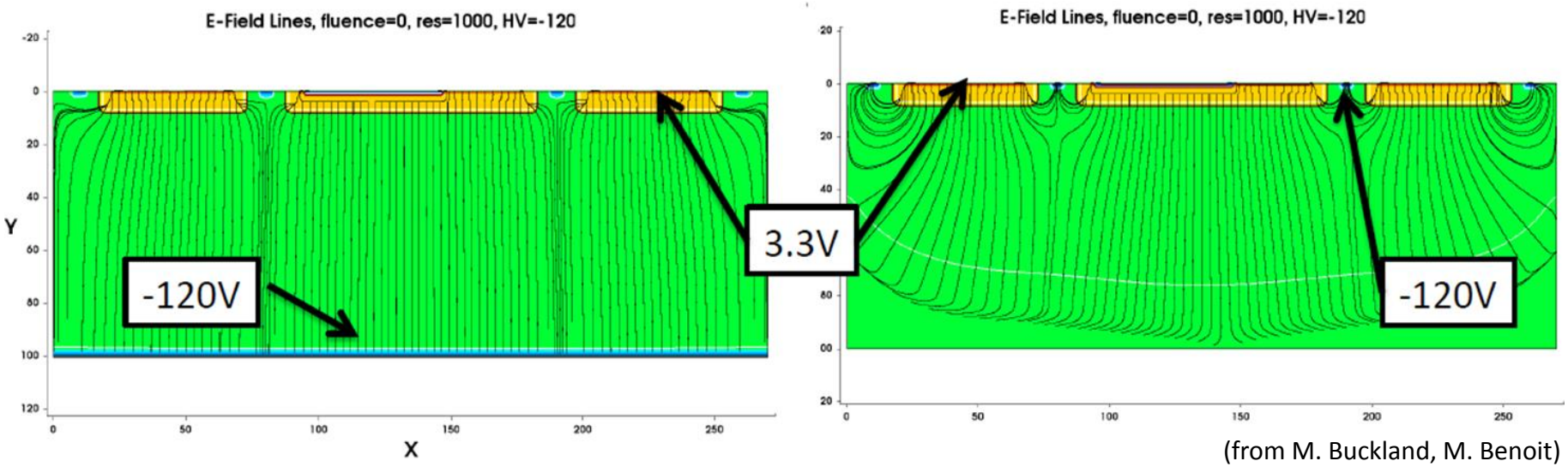
2nd analog matrix:

- CSA uses pMOS as input transistor
- First 100 columns with extra HV
- First 200 columns with gain boosting
- Last 100 columns without gain boosting

Pixel area | **FE-I4**

TCAD simulations

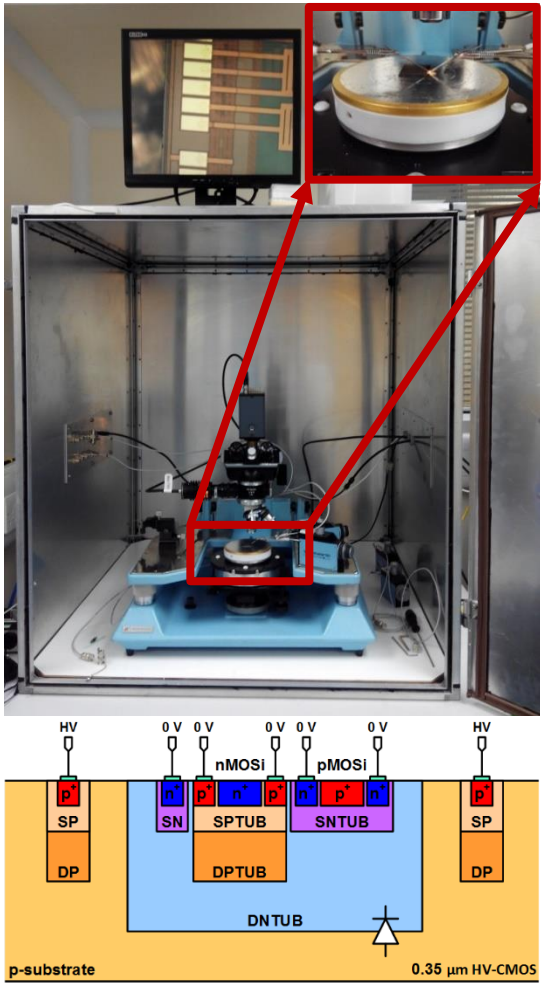
- **Backside biasing versus top-side biasing:**



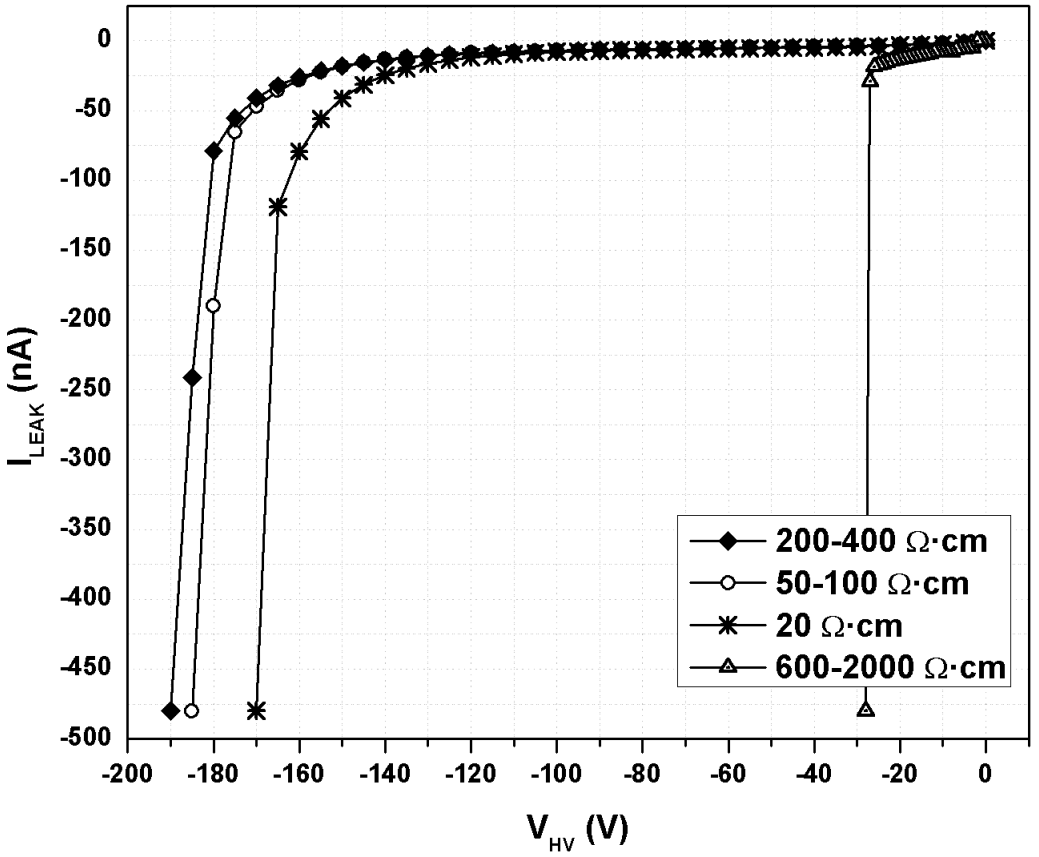
(from M. Buckland, M. Benoit)

- Backside biasing gives a more uniform field.
- As AMS doesn't provide backside biasing, we plan to do backside processing on our fabricated H35DEMO devices at a third company.

H35DEMO - I-V measurements



Liverpool probe station in clean room

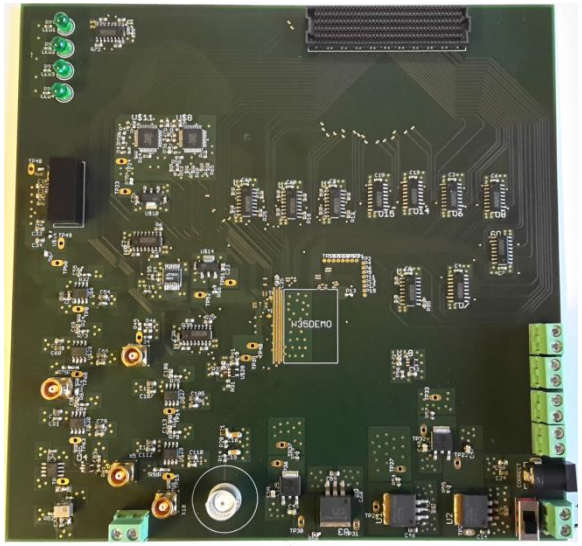


$I_{LEAK} < 10$ nA

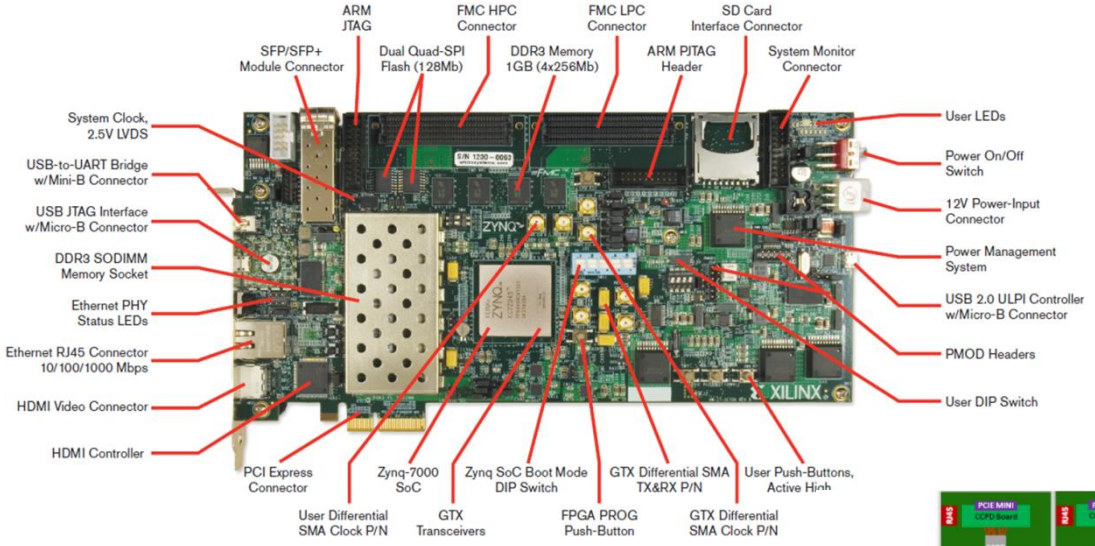
$I_{LEAK} < 2.2$ nA/cm^2

H35DEMO - Measurement set-up

Set-up being developed @ Liverpool

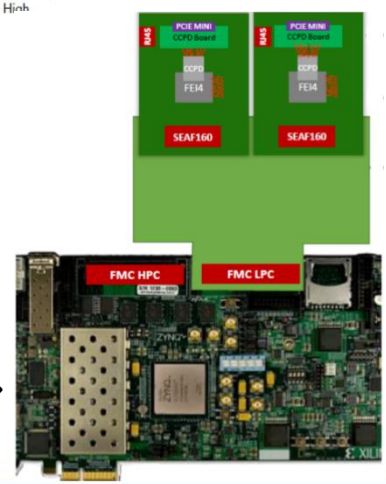


PCB designed @ Liverpool



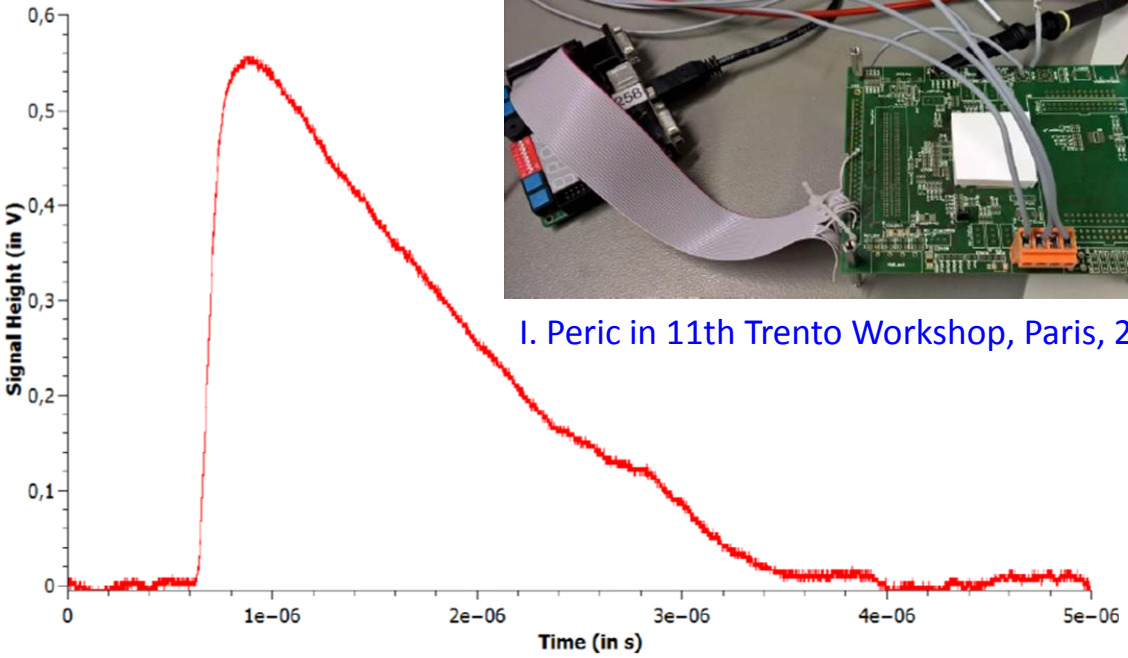
Xilinx ZC706 Evaluation Kit

- PCB especially designed to test the standalone nMOS matrix
- No attachment to FE-I4 with this test board
- LVDS links to FPGA through FMC connector
- ~ 60 I/O connections to FPGA
- Plans to use the Caribou readout system (Brookhaven and Uni. Geneva) →
- **On-going work**



H35DEMO - Preliminary measurements

- On-going measurements in parallel at different institutes:



I. Peric in 11th Trento Workshop, Paris, 2016

Features:

- **Sr90 source**
- **1st analog matrix**
- **Monitor line**

- University of Lancaster → Edge TCT on test structures

LFoundry 150 nm

- The design of an HV-CMOS prototype in LFoundry 150 nm is currently on-going
- The prototype will include matrices with different features:
  - **Matrix 1 → High rate readout with trigger and based on associative buffer cells**
  - **Matrix 2 → High rate readout based on shift register**
  - **Matrix 3 → Analog pixels**
  - **Matrix 4 → High rate readout with Time-to-Digital Converter circuits**
    - Push the time resolution of the sensor (for Mu3e and also interesting for ATLAS)
    - Very small area pixels
- Prototype area will be 1 cm x 1 cm (MPW)
- Thinning, backside biasing and fabrication in different substrate resistivities (HR) are foreseen
- Development of this prototype also in collaboration with other institutes: IFAE, KIT, University of Bern, University of Geneva and University of Liverpool
- Submission of this prototype will be in June 2016
- We target 2 other submissions later in 2016 → 1. Engineering run in HV-AMS 180 nm
  2. Engineering run in LFoundry 150 nm

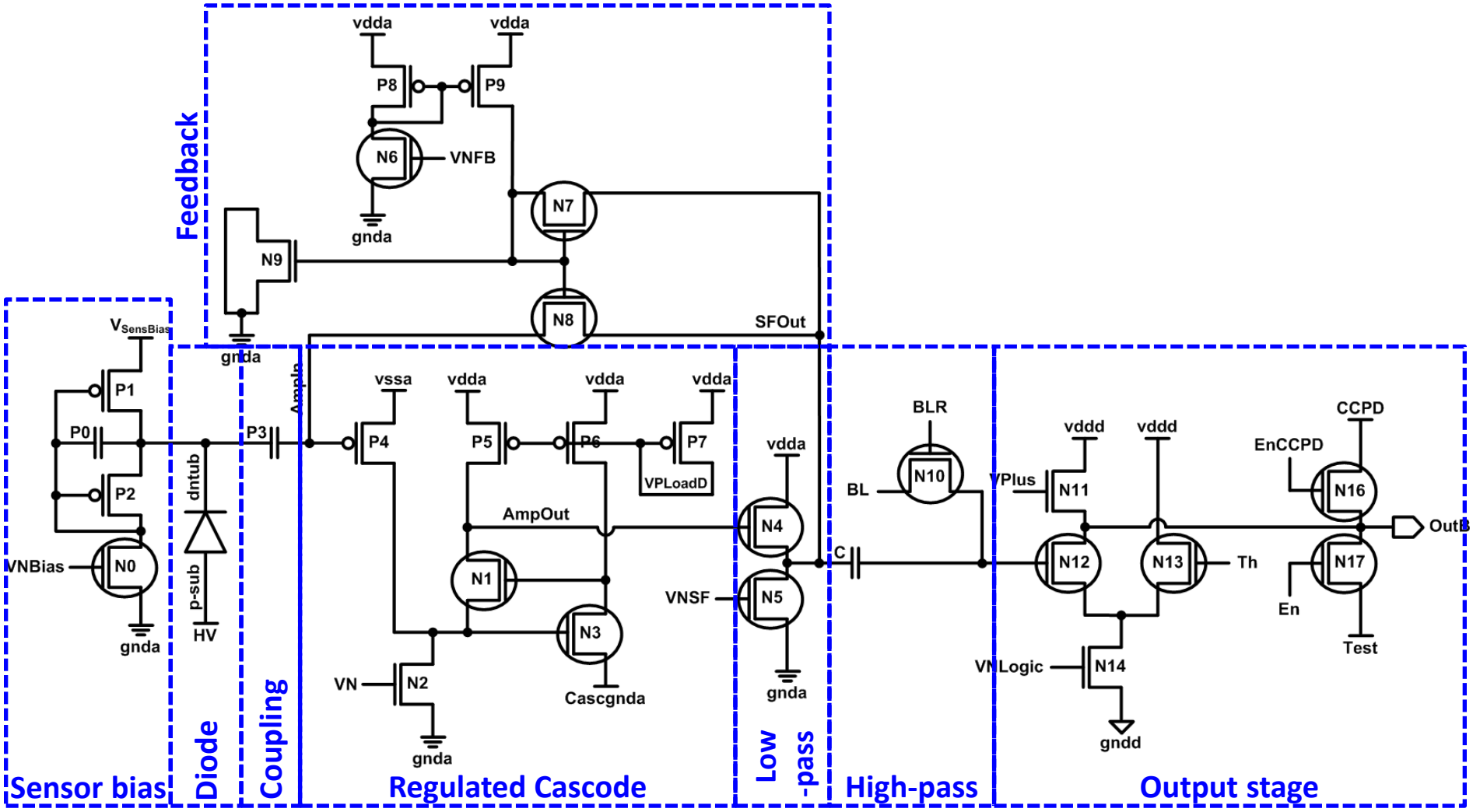
Conclusion

- **MAPS sensors** offer very attractive advantages and have demonstrated excellent performance, but they are not suited for certain future HEP experiments in terms of speed and radiation tolerance.
- **HV-CMOS/HV-MAPS** add to MAPS sensors advantages high speed (charge collection via drift) and advanced radiation tolerance.
- Many HV-CMOS/HV-MAPS developments **in a few different technologies** (mostly in HV-AMS 0.35 µm/180 nm and LFoundry 150 nm, but also in ESPROS 150 nm, XFAB 180 nm, TJ 180 nm and others) **aiming at various applications** (ATLAS upgrade, Mu3e and ILC/CLIC) **and by several groups**.
- Liverpool has started an **R&D programme to develop HV-CMOS sensors**:
  - Design and fabrication of a **pixel demonstrator in HV-AMS 0.35 µm (H35DEMO)**
  - I-V measurements done with probe station in clean room at Liverpool
  - Development of experimental set-up is on-going at different institutes
  - Future plans with H35DEMO include thinning and back processing, bump bonding and gluing with FE-I4, but also irradiation measurements and test beam campaigns
  - Design of a prototype in LFoundry 150 nm

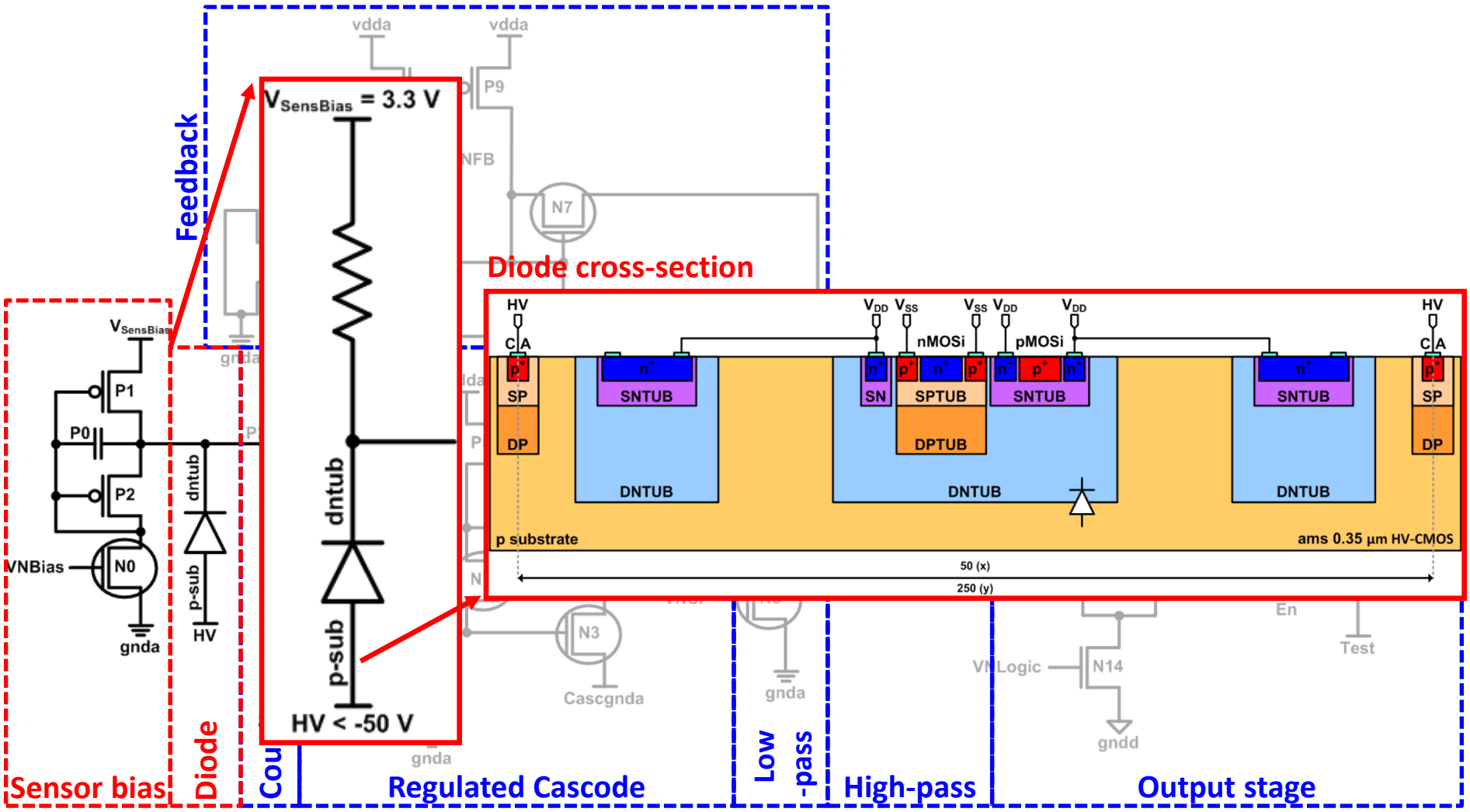
Thank you for your attention!

Back-up slides

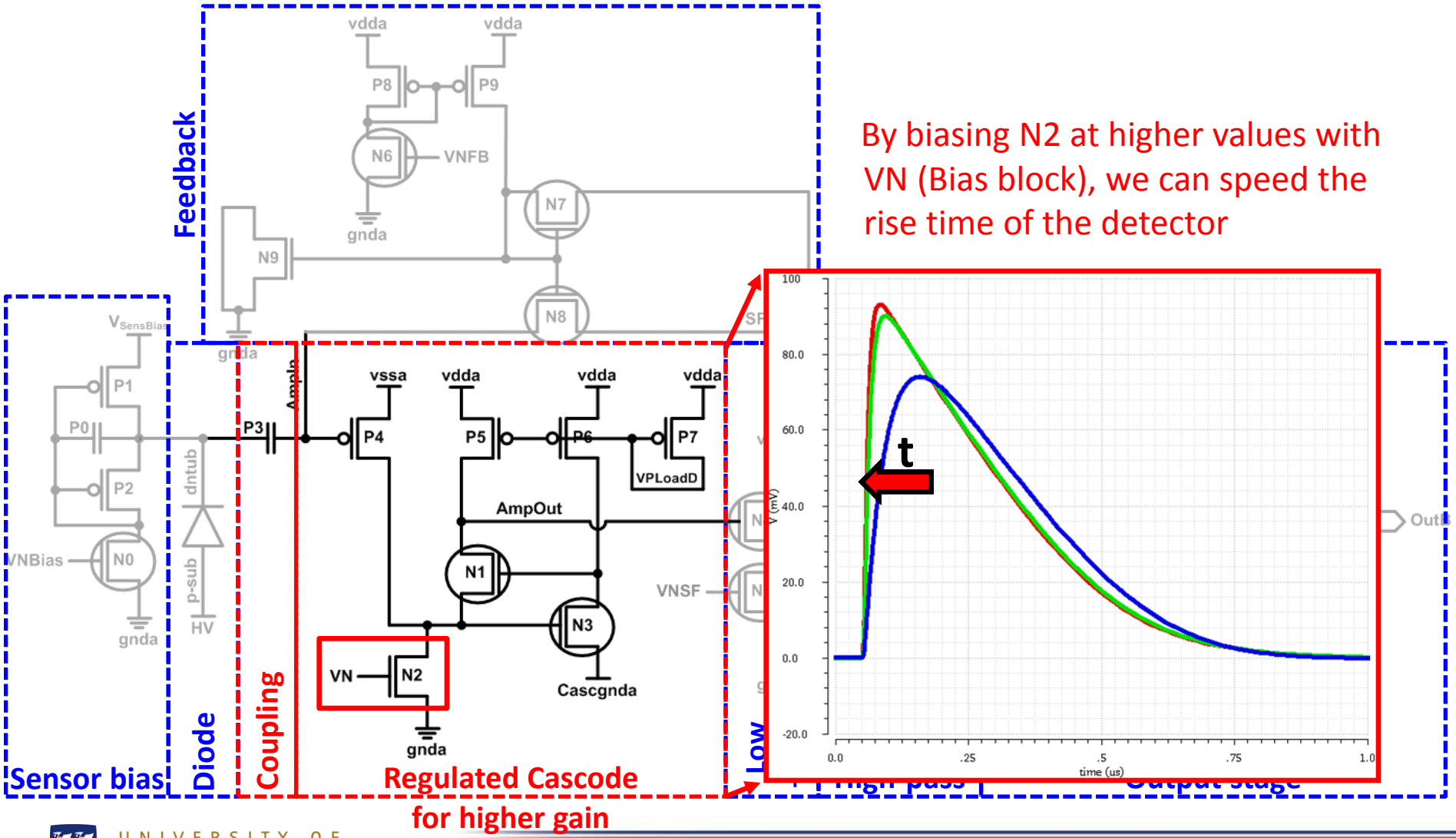
H35DEMO - Schematic analog pixel



H35DEMO - Schematic analog pixel

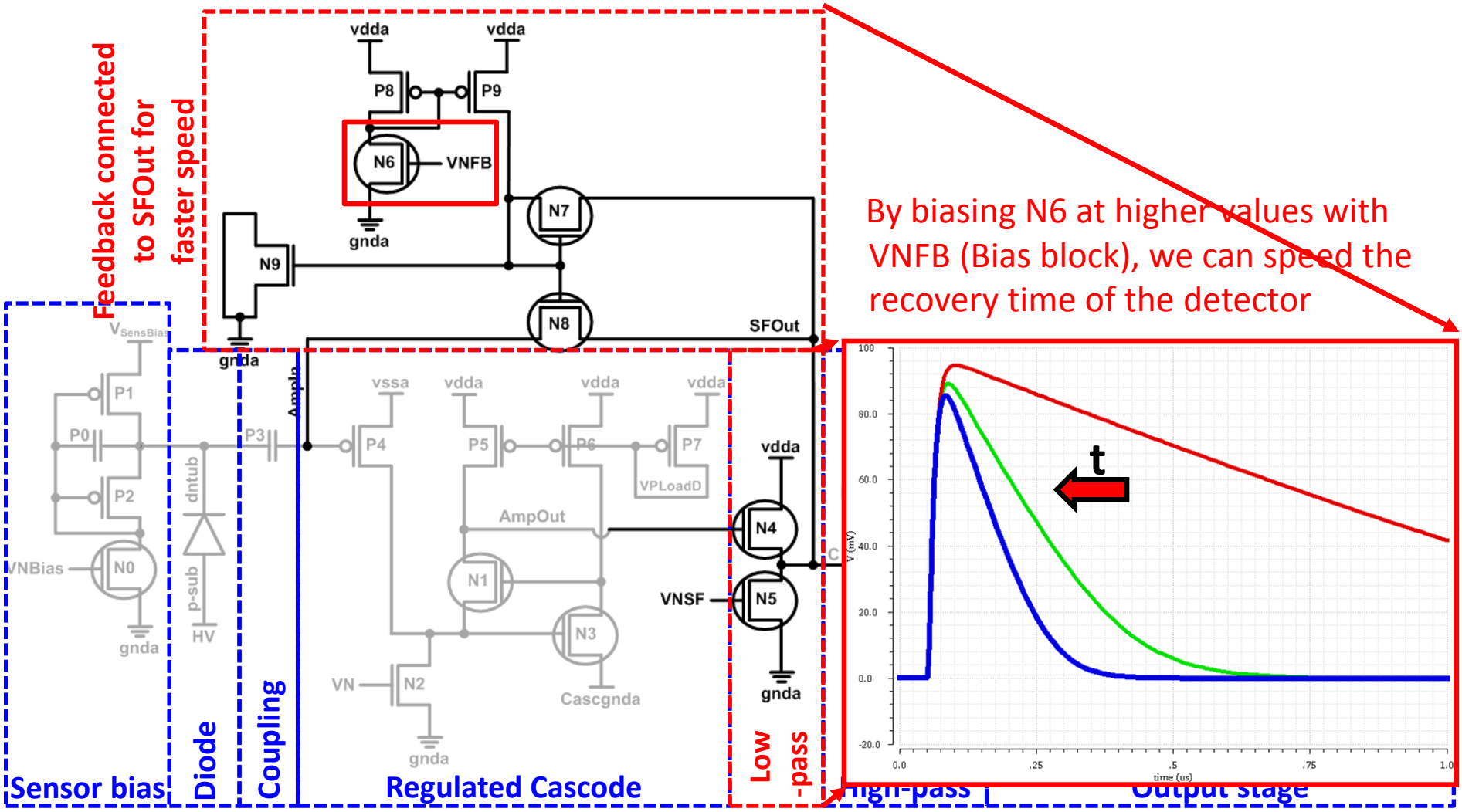


H35DEMO - Schematic analog pixel

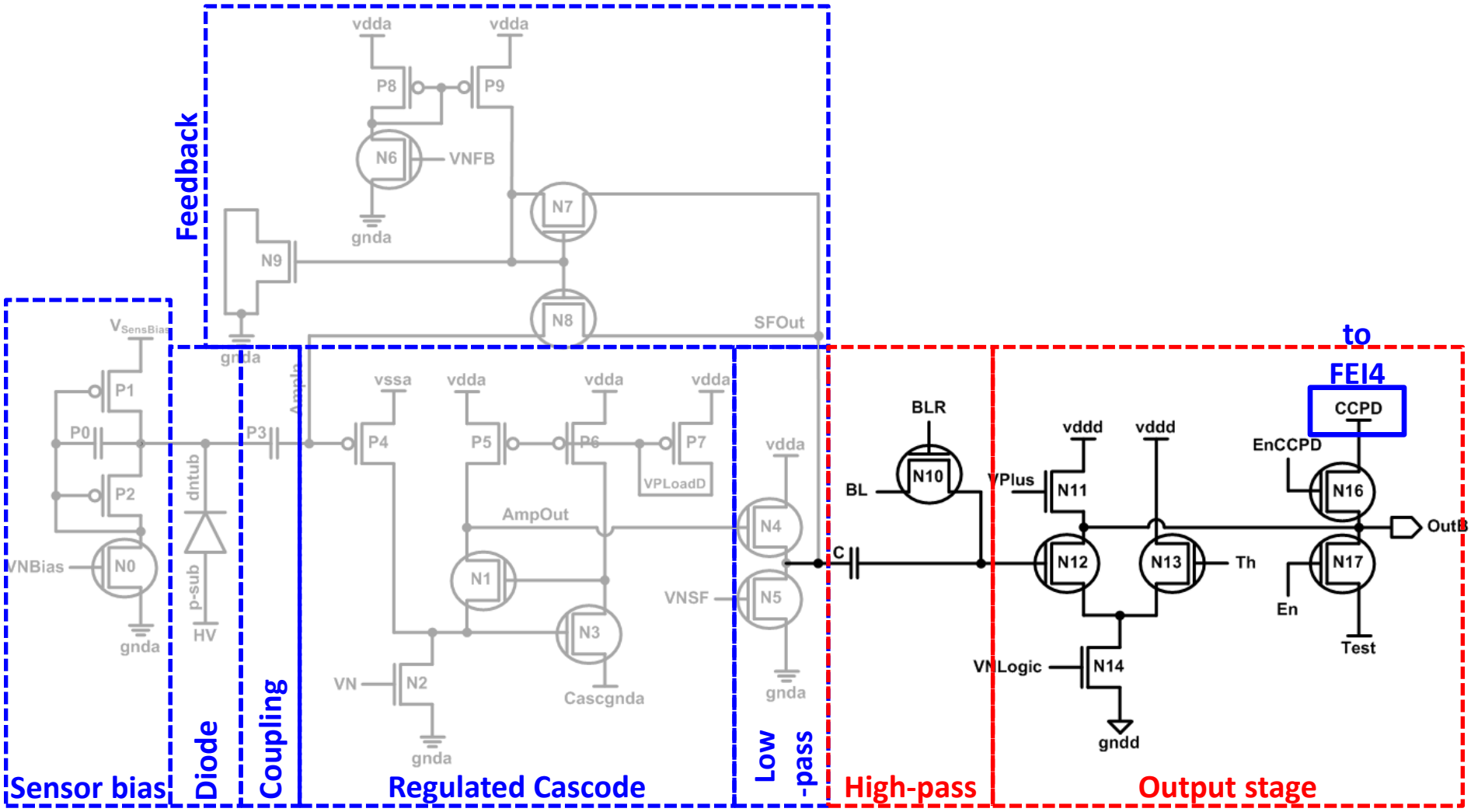


By biasing N2 at higher values with VN (Bias block), we can speed the rise time of the detector

H35DEMO - Schematic analog pixel



H35DEMO - Schematic analog pixel



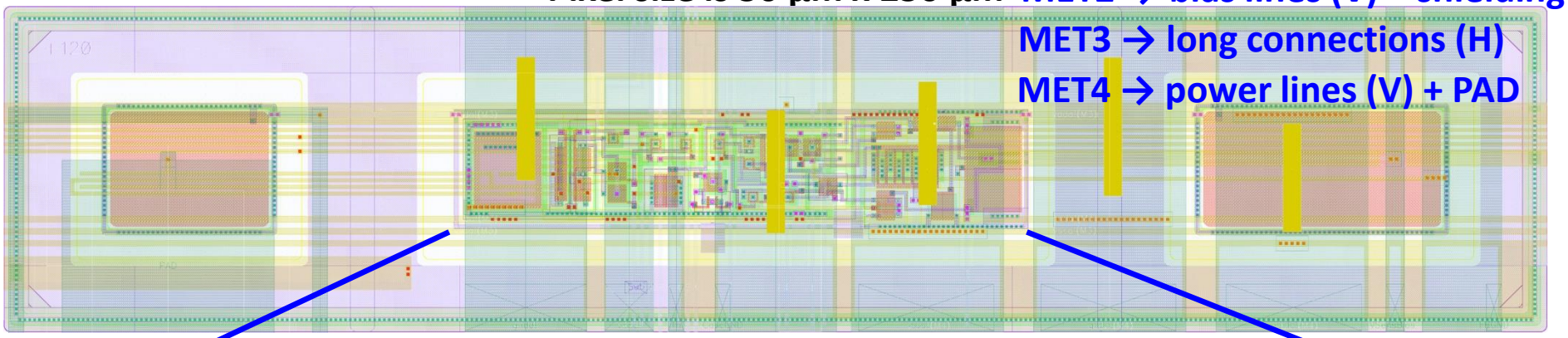
H35DEMO - Layout analog pixel

MET1 → in-pixel connections

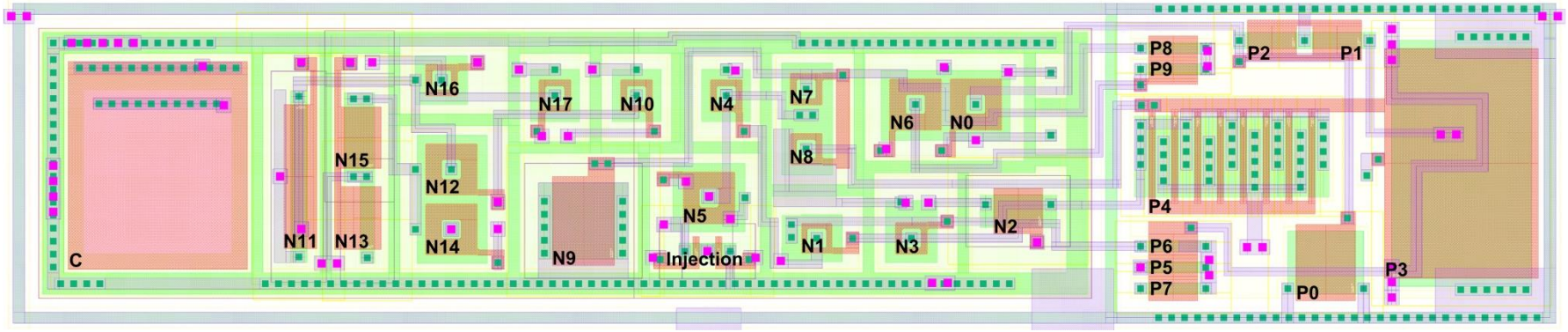
Pixel size is 50 µm x 250 µm MET2 → bias lines (V) + shielding

MET3 → long connections (H)

MET4 → power lines (V) + PAD

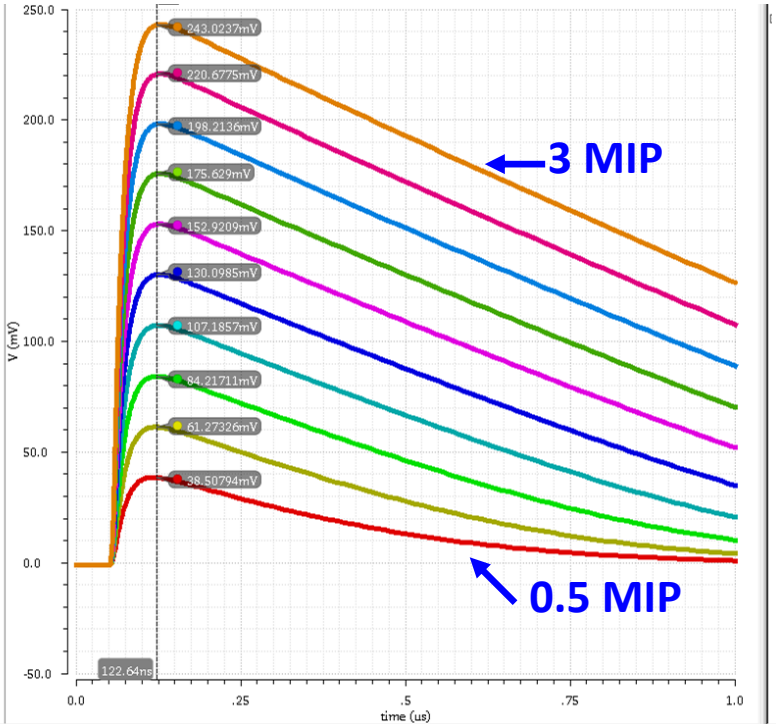


Transistors area is 20.25 µm x 95.05 µm

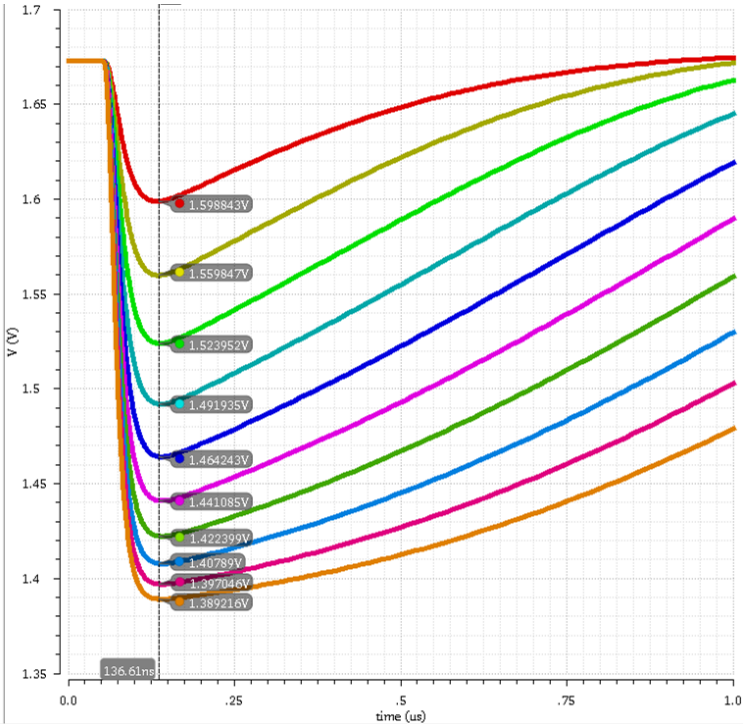


H35DEMO - Post-layout simulation

SFOut



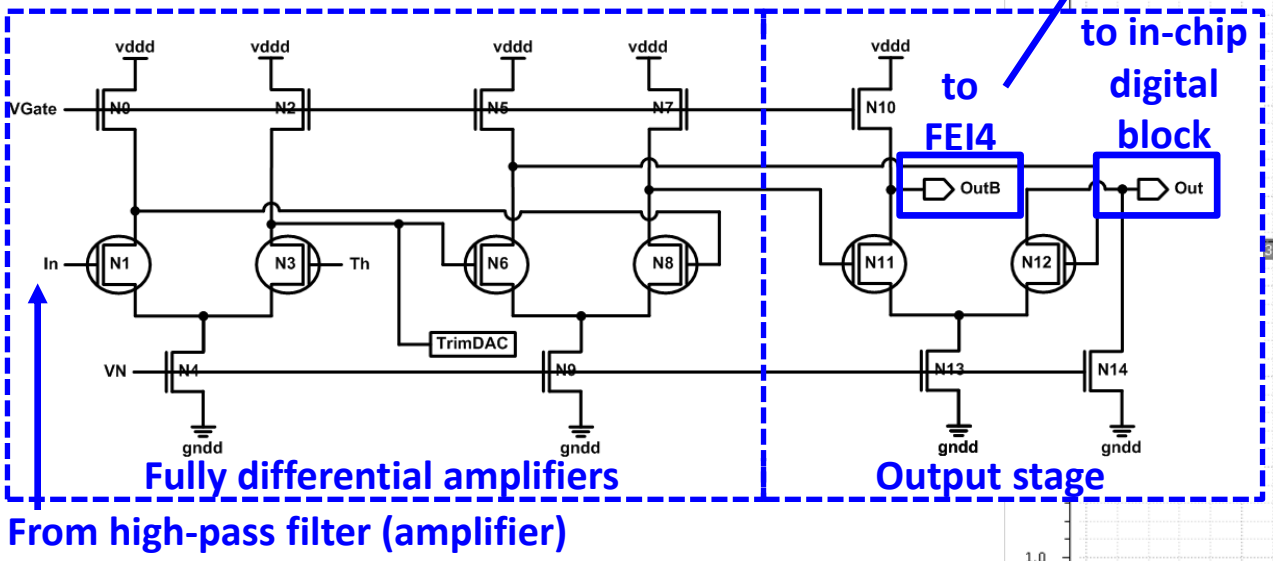
CCPD

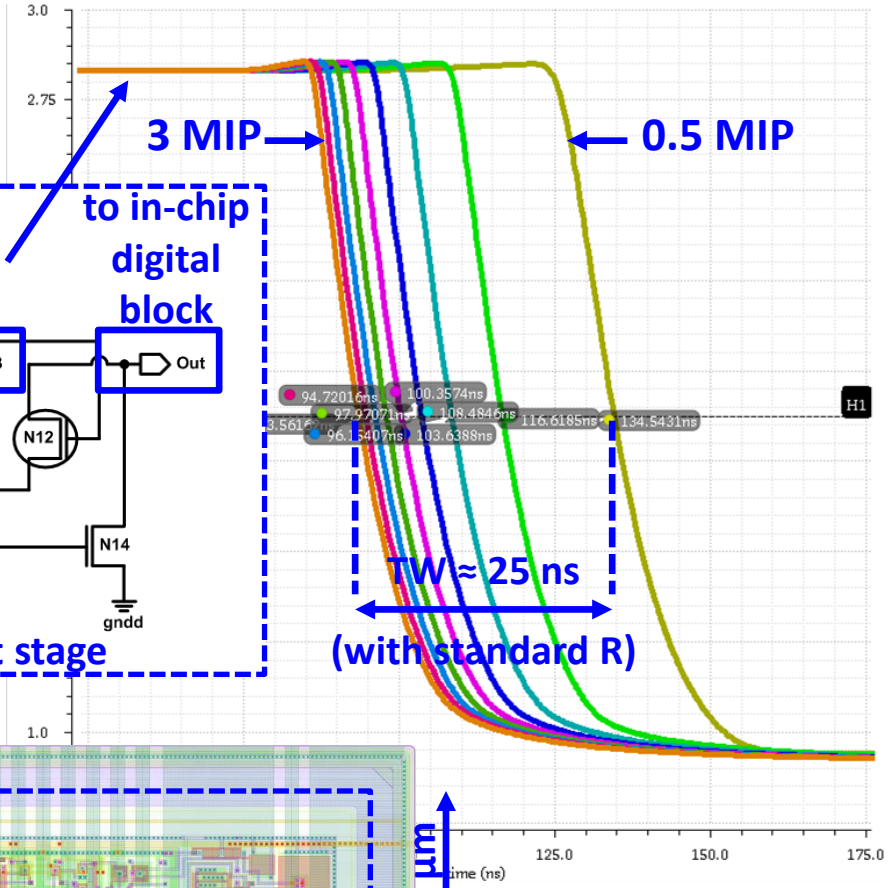


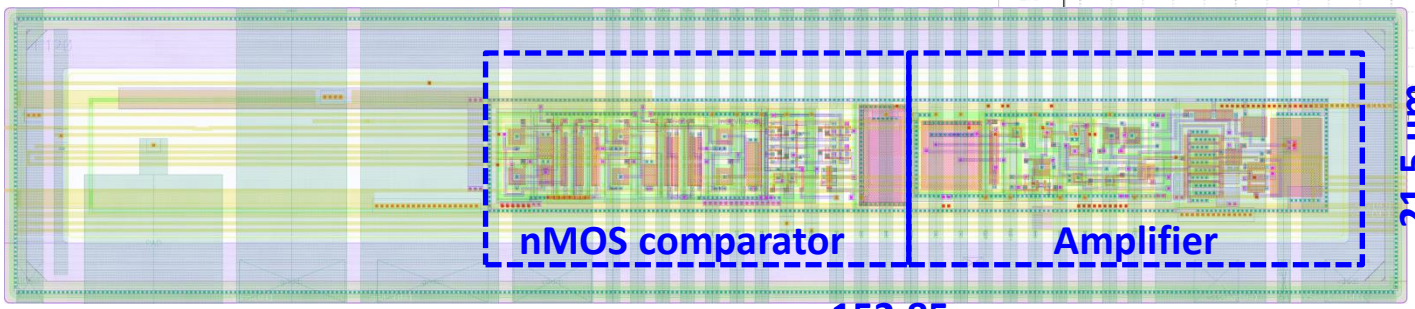
- The gain ranges between 38 mV (0.5 MIP) and 243 mV (3 MIP).
- The rise time is ≈ 31 ns.
- The recovery time ranges between ≈ 600 ns (0.5 MIP) and ≈ 1.6 µs (3 MIP). It can be reduced to ≈ 80-100 ns with more aggresive settings.
- The noise is 8 mV.

H35DEMO - Standalone nMOS pixel

- All nMOS comparator (in-pixel):







H35DEMO - Standalone nMOS pixel TW free

- All nMOS comparator (in-pixel):

- Fully differential amplifiers
- Compensation system
- Output stage
  - To FEI4
  - To in-chip digital block