Detector R&D for a CLIC Vertex Detector

HEP seminar
University of Liverpool
January 22nd, 2014

Dominik Dannheim (CERN-LCD)
on behalf of the
CLIC detector and physics study

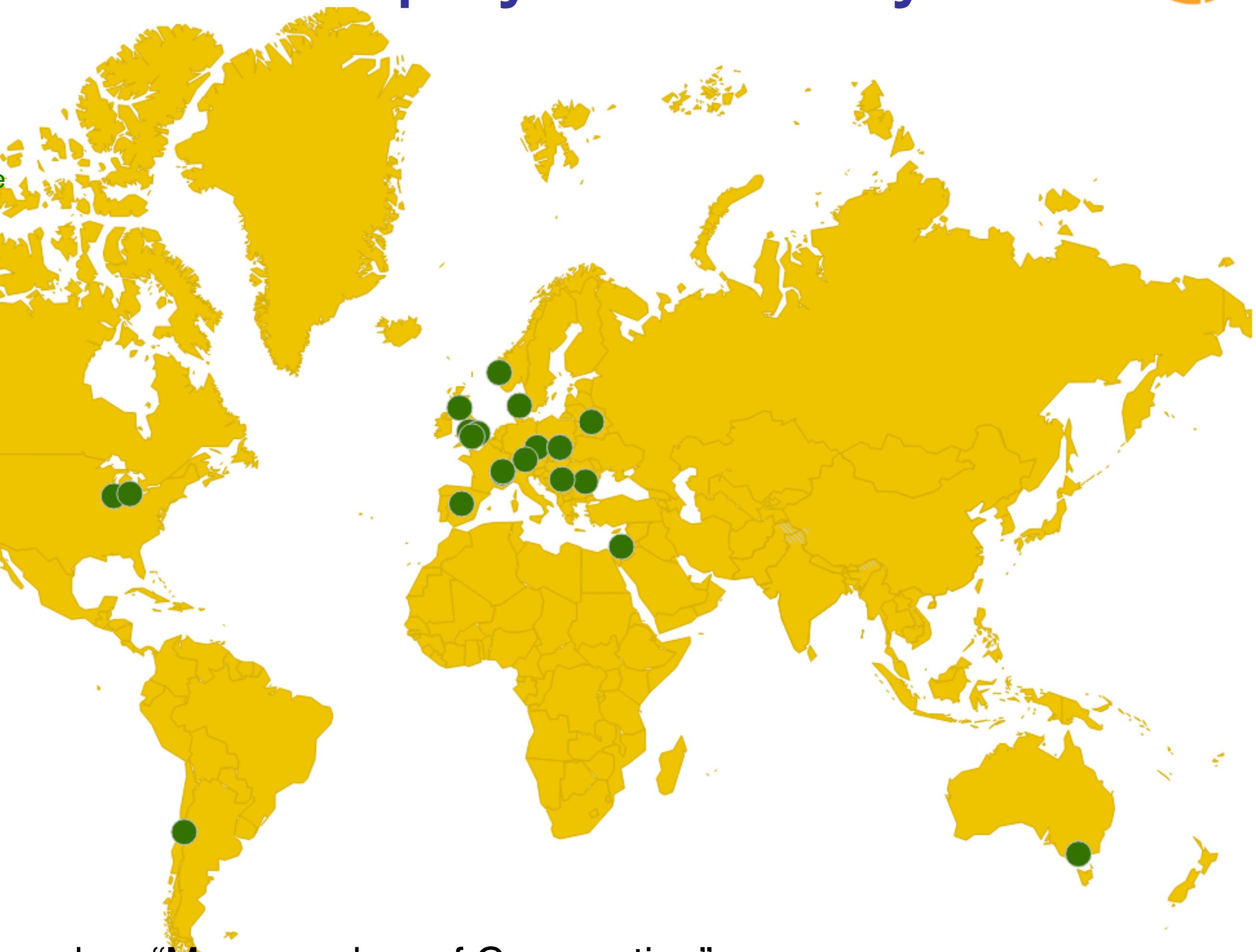
Outline

- CLIC physics and accelerator
- Vertex-detector requirements
- Detector optimization studies
- R&D on sensors and readout
- Powering, cooling and detector integration
- Summary / Conclusions

CLIC detector & physics study

CLICdp member institutes

- Dept. of Physics, Aarhus University
- Laboratoire d'Annecy-le-Vieux de Physique des Particules (LAPP), Annecy
- Vinca Institute for Nuclear Sciences, Belgrade
- University of Bergen
- The School of Physics and Astronomy, University of Birmingham
- Institute of Space Science, Bucharest
- Dept. of Physics, University of Cambridge
- Dept. of Physics and Technology, AGH University of Science and Technology, Cracow
- Polish Academy of Sciences, Cracow
- CERN, Geneva
- University of Glasgow
- Argonne National Laboratory, Lemont
- Australian Collaboration for Accelerator Science (ACAS), Melbourne
- University of Michigan, Ann Arbor
- NC PHEP, Belarusian State University, Minsk
- MPI Munich
- Dept. of Physics, Oxford University
- Institute of Physics of the Academy of Sciences of the Czech Republic, Prague
- Pontificia Universidad Católica de Chile, Santiago de Chile
- Spanish Network for Future Linear Colliders
- Dept. of Physics, Tel Aviv University



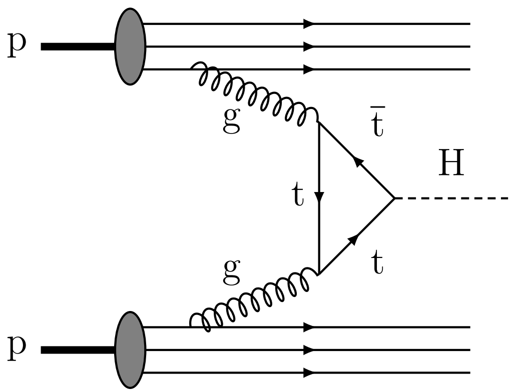
•Pre-collaboration structure based on "Memorandum of Cooperation": http://lcd.web.cern.ch/lcd/Home/MoC.html

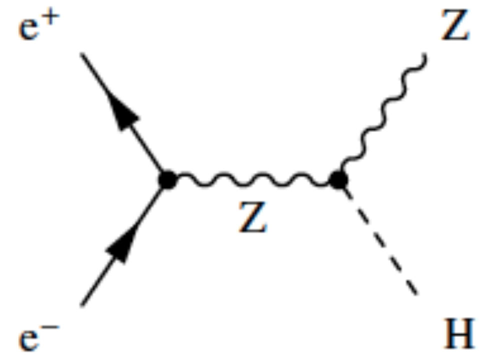
•CERN acts as host laboratory

•Currently 21 institutes from 16 countries, more contributors most welcome!

•The CLIC accelerator R&D is being conducted in collaboration with ~48 institutes

Hadron vs. lepton colliders



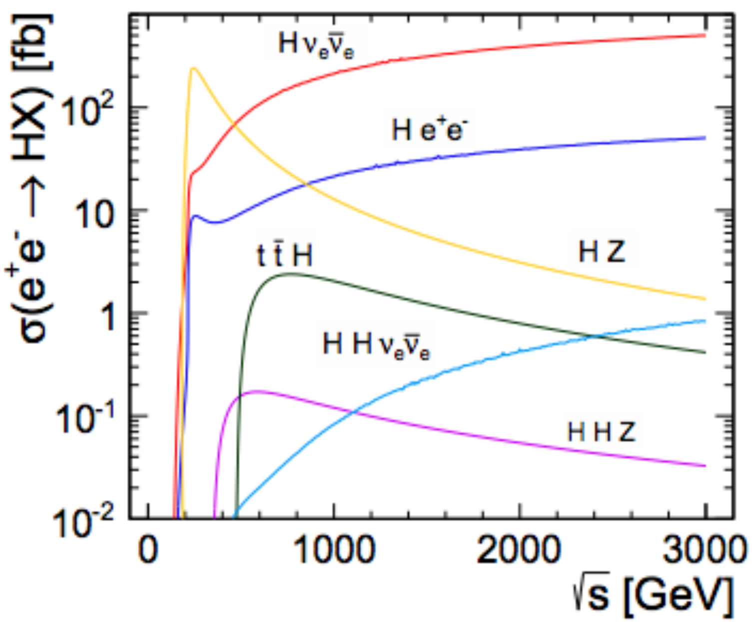


p-p collisions	e^+e^- collisions
Proton is compound object → Initial state not known event-by-event → Limits achievable precision	e^+/e^- are point-like → Initial state well defined (√s / polarization) → High-precision measurements
Circular colliders feasible	Linear Colliders (avoid synchrotron rad.)
High rates of QCD backgrounds → Complex triggering schemes → High levels of radiation	Cleaner experimental environment → trigger-less readout → Low radiation levels
√s constrained by design	√s can be tuned → Threshold scans
High cross-sections for colored-states	Superior sensitivity for electro-weak states

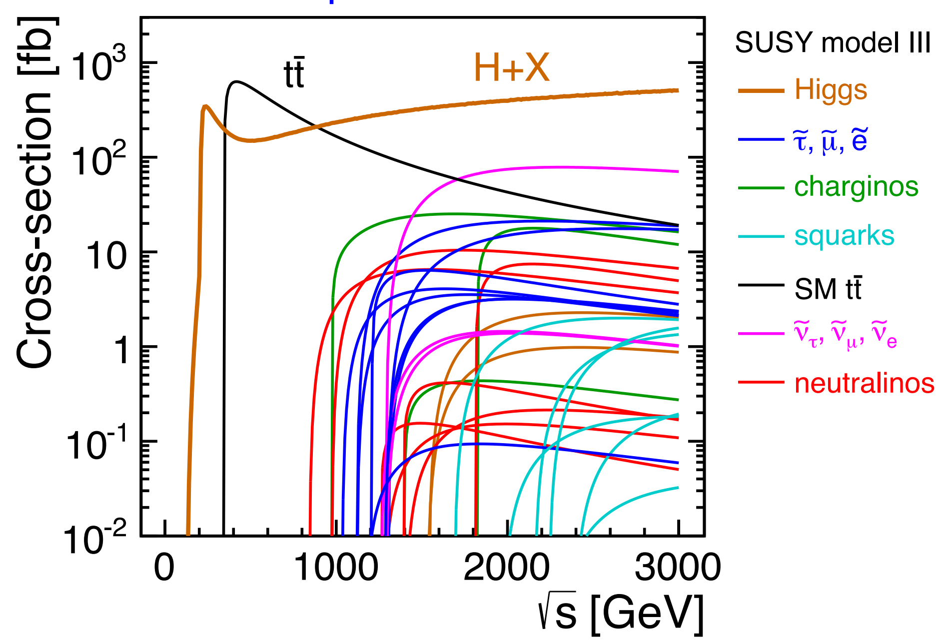
CLIC physics program

- CLIC: linear e^+e^- collider concept, $\sqrt{s}$ from few hundred GeV up to 3 TeV
- Physics goals:
  - Precision measurements of SM processes (Higgs, top)
  - Precision measurements of new physics potentially discovered at 14 TeV LHC
  - Search for new physics: unique sensitivity to particles with electroweak charge

Higgs



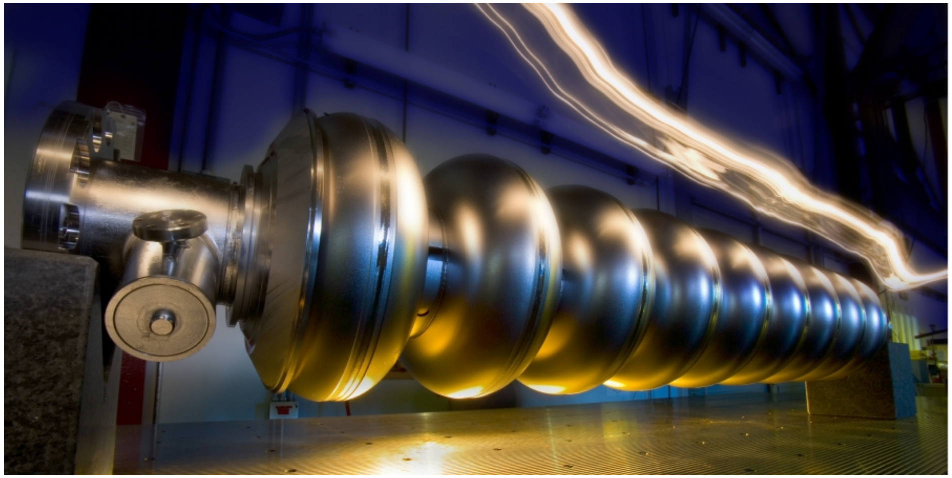
SUSY example scenario



ILC and CLIC

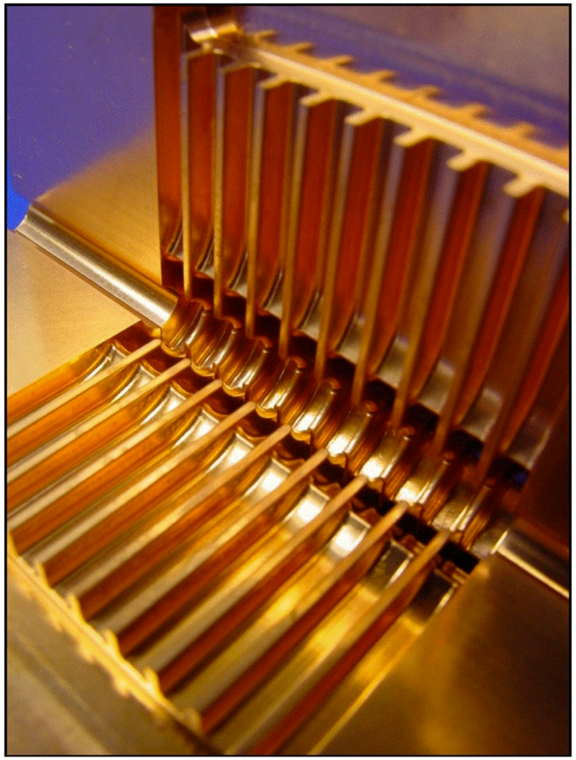
- Linear e^+e^- colliders
- Luminosities: few 10^{34} $cm^{-2}s^{-1}$

ILC



•superconducting RF cavities (like XFEL)
•Gradient 32 MV/m
•$\sqrt{s} \leq 500$ GeV (1 TeV upgrade option)
•Focus on ≤ 500 GeV, ongoing studies for 1 TeV

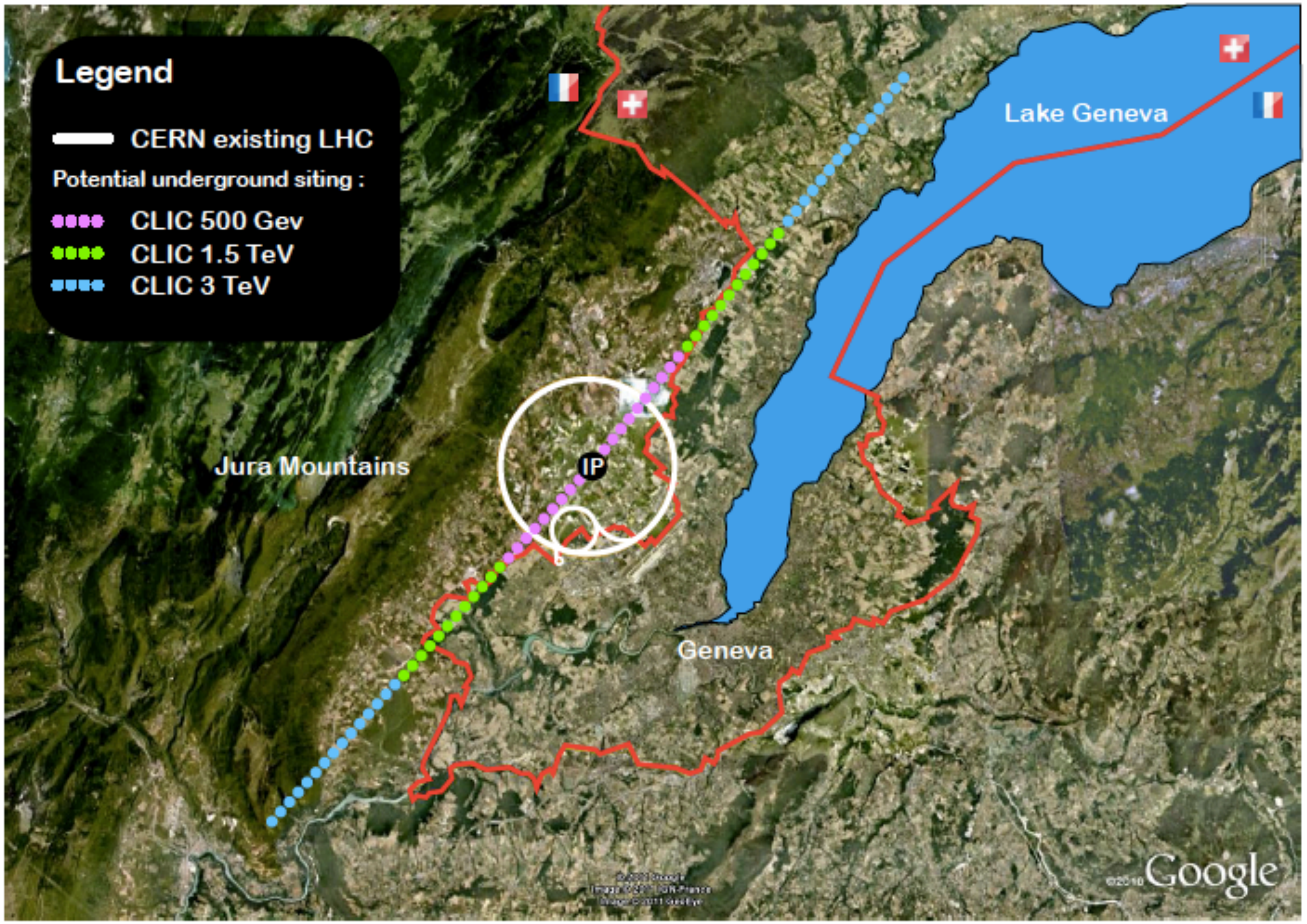
CLIC



•2-beam acceleration scheme operated at room temperature
•Gradient 100 MV/m
•$\sqrt{s}$ up to 3 TeV
•Physics + Detector studies for 350 GeV - 3 TeV

CLIC implementation

- Example of staged CLIC implementation underground near CERN
- ~48 km tunnel length for 3 TeV stage
- The site specifications do not constrain the implementation to this location

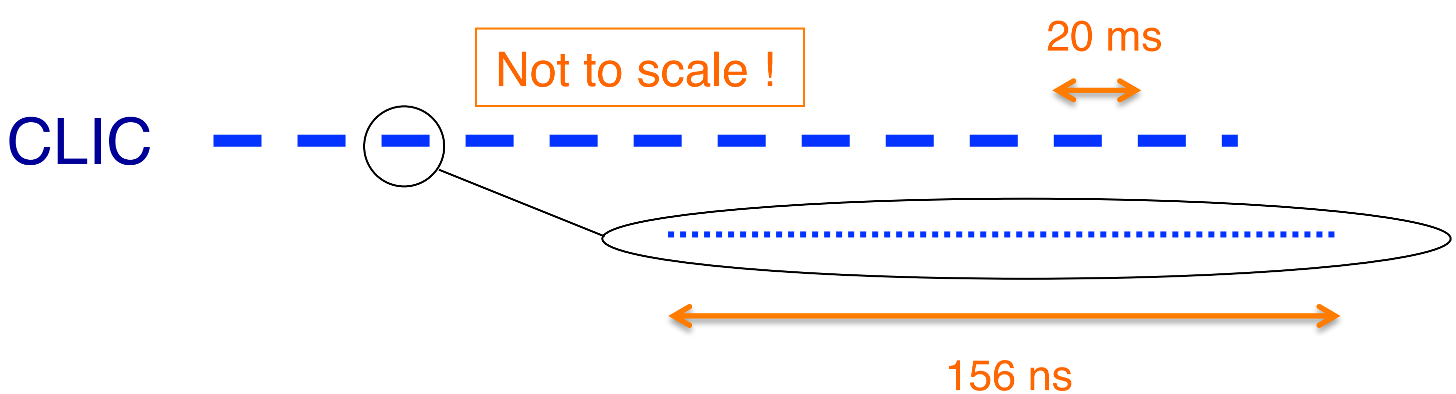


Machine parameters

	LHC at 14 TeV	ILC at 500 GeV	CLIC at 3 TeV
L ($cm^{-2}s^{-1}$)	$1x10^{34}$	$2x10^{34}$	6×10^{34}
BX separation	25 ns	554 ns	0.5 ns
#BX / train	2808	1312	312
Train duration	70 µs	727 µs	156 ns
Train repetition	14 kHz	5 Hz	50 Hz
Duty cycle	~1	0.36%	0.00078%
σ_x / σ_y [nm]	15000 / 15000	474 / 6	≈ 45 / 1
σ_z [µm]	~50000	300	44

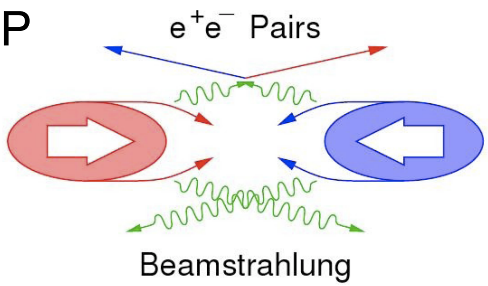
drives timing requirements for detectors

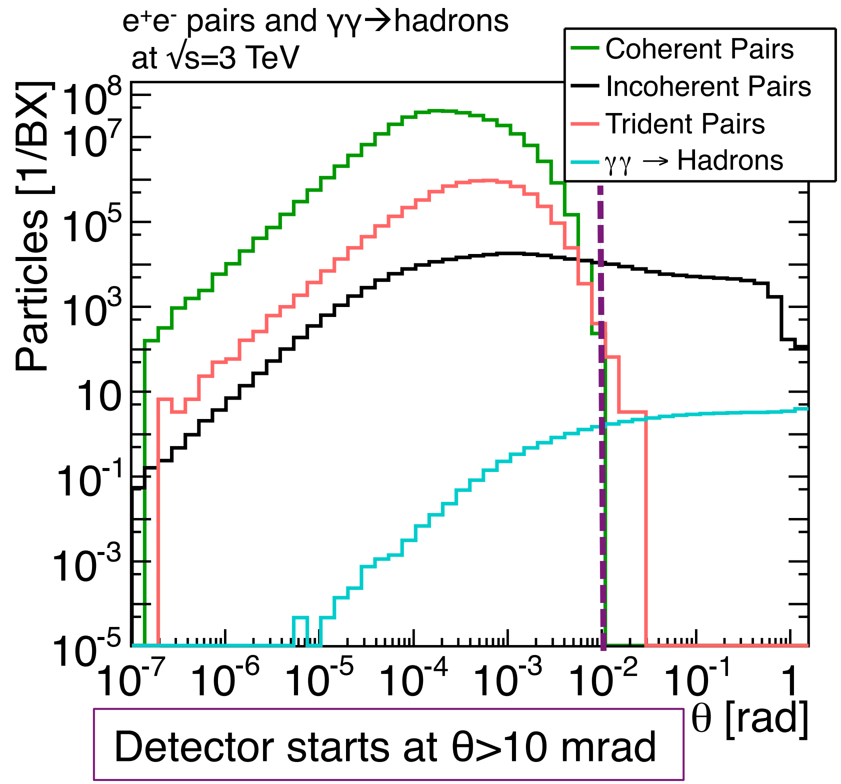
very small beam sizes at interaction point

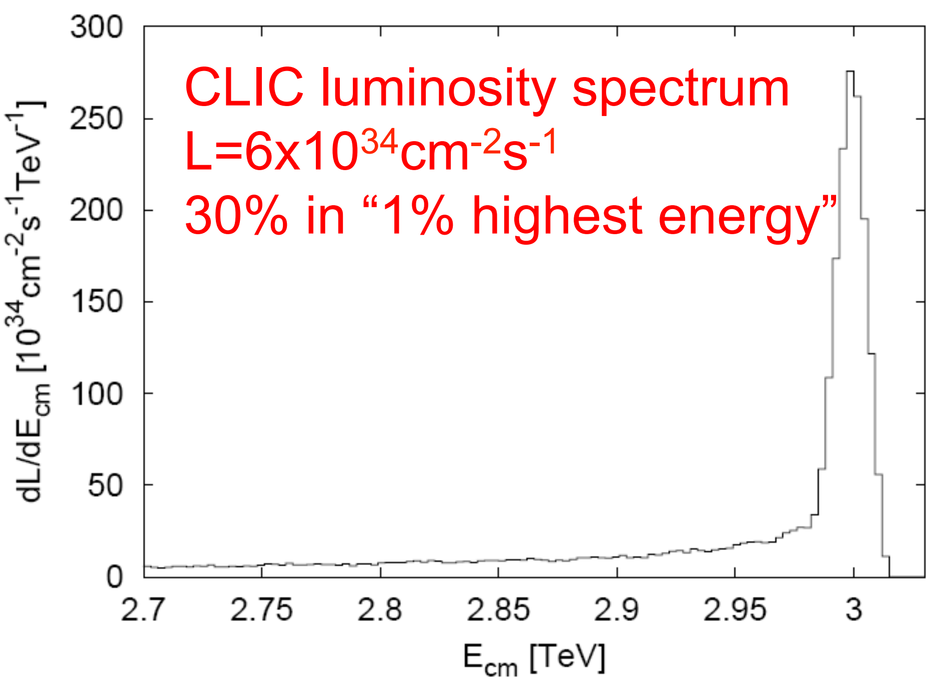


Beam-induced backgrounds

small beam profiles at IP
→very high E-fields
Beamstrahlung
leads to:
• e^+e^- pairs
• hadronic events
→ Reduces E_{cm}
→ Background particles



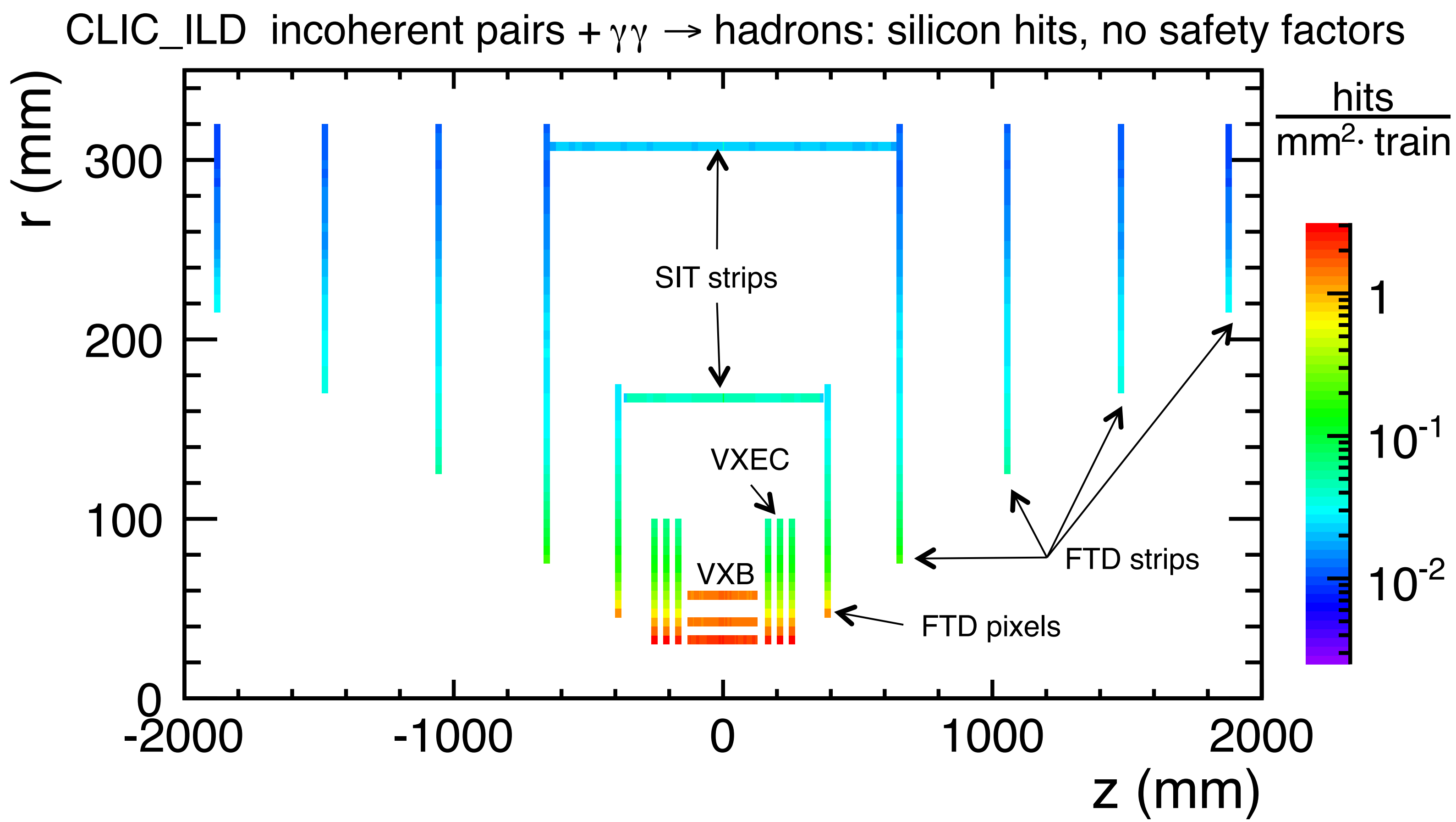




Main backgrounds in detector:
- **Incoherent e^+e^- pairs**: 60 particles / BX
  detector design issue (occupancies)
- **γγ→hadrons**: 54 particles / BX
  impacts physics

→ Need **pile-up rejection**

Backgrounds in inner tracking region



- Train occupancies up to 3% in vertex region (including clustering and safety factors)
- moderate radiation exposure, ~10^4 below LHC

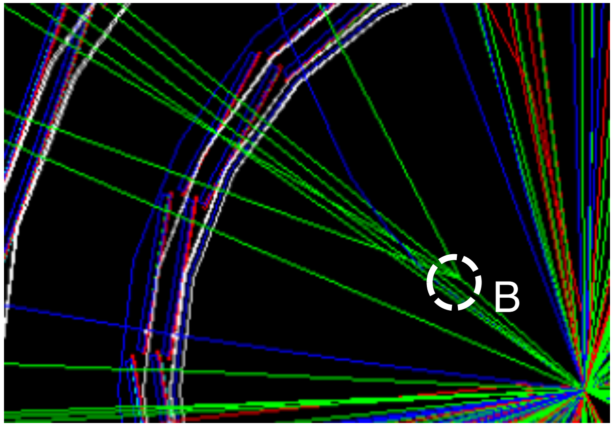
Region	Readout granularity	Max. occup.	NIEL [$n_{eq}/cm^2/y$]	TID [Gy/y]
VXB	20 µm x 20 µm	1.9 %	$4x10^{10}$	200
VXEC	20 µm x 20 µm	2.8 %	$5x10^{10}$	180
FTD pixels	20 µm x 20 µm	0.6%	$2.5x10^{10}$	50
FTD strips	10 cm x 50 µm	290 %	$1x10^{10}$	7
SIT	9 cm x 50 µm	170 %	$2x10^9$	2

Vertex-detector requirements

- Efficient tagging of heavy quarks through precise determination of displaced vertices:

$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot \mathrm{GeV}^2/(p^2 \sin^3\theta)}$$

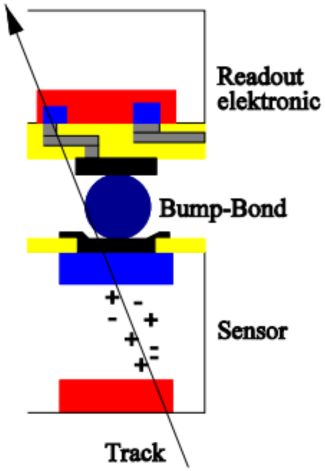
$a \sim 5\ \mu m,\ \ b \sim 15\ \mu m$



→ good single point resolution: $\sigma_{SP} \sim 3\ \mu m$
  → small pixels ~25x25 μm^2, analog readout
→ low material budget: $X \lesssim 0.2\%\ X_0$ / layer
  → corresponds to ~200 µm Si, including supports, cables, cooling
  → low-power ASICs (~50 mW/cm^2) + gas-flow cooling

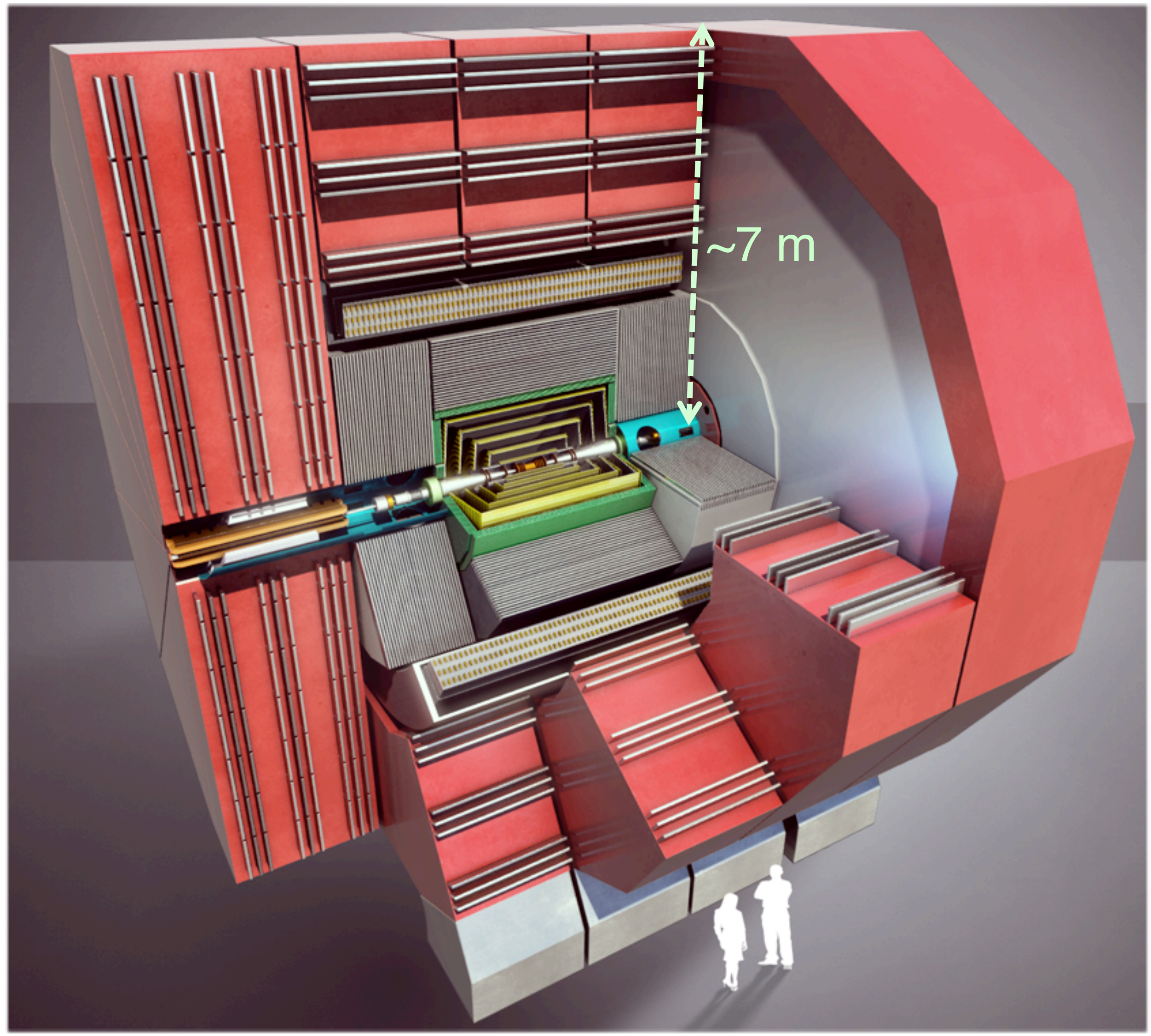
- Time slicing with ~10 ns accuracy, to suppress beam-induced backgrounds
  → High-resistivity sensors, fast readout
  → Hybrid concept (like for LHC detectors):
    ultra-thin sensors
    + high-performance r/o ASICs

Hybrid pixel technology



CLIC detector concepts

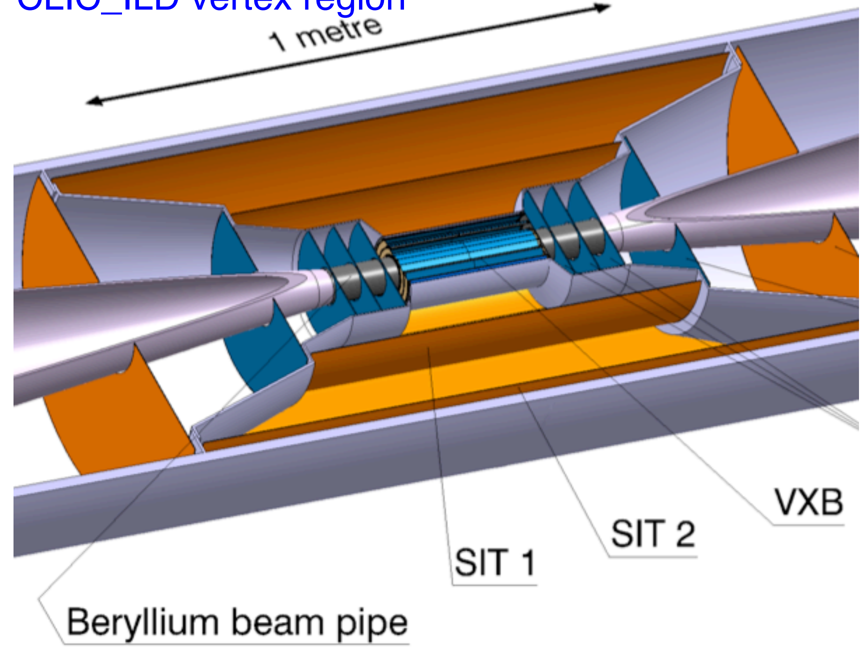
CLIC_ILD & CLIC_SiD
- detector concepts based on concepts developed for International Linear Collider (ILC):
- low-mass **vertex detector** with ~25x25 μm^2 pixels
- **main trackers**: TPC + silicon (CLIC_ILD) or all silicon (CLIC_SiD)
- fine-grained **PFA calorimetry**, 1+7.5 Λ_i
- 4-5 T **solenoids**
- **return yoke** instrumented for muon ID
- complex **forward region** with final beam focussing



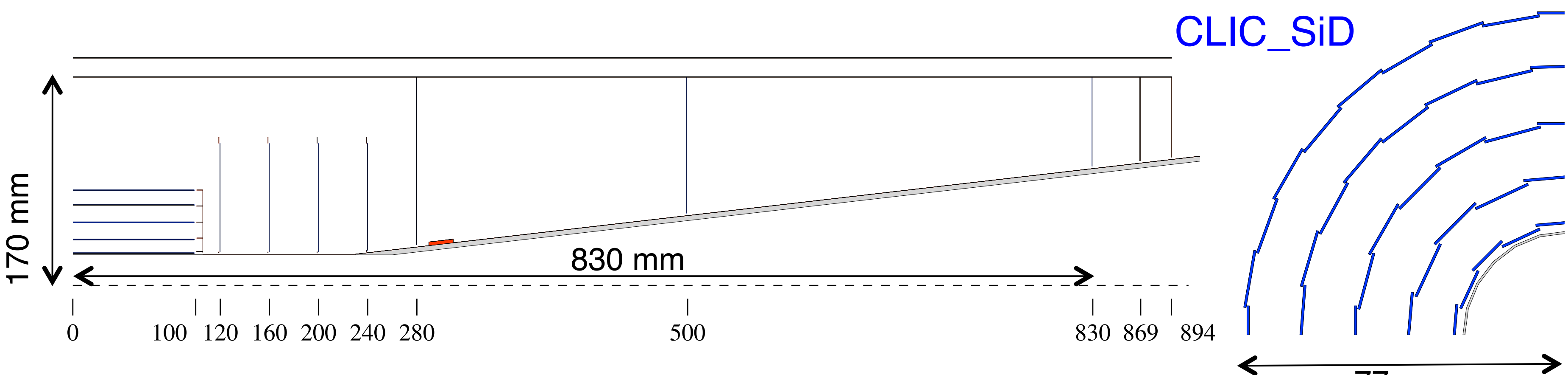
Vertex-detector concepts

- barrel/end-cap layout
- 3 double layers or 5 single layers in central region
- 3 double layers or 7 single layers in forward region (θ>7°)
- ~25x25 μm² pixel size
- ~1 m² area, ~2 Gpixels
- R_i ~ 27-31 mm
- beam pipes with conical sections
- optimized for high performance and low background occupancy

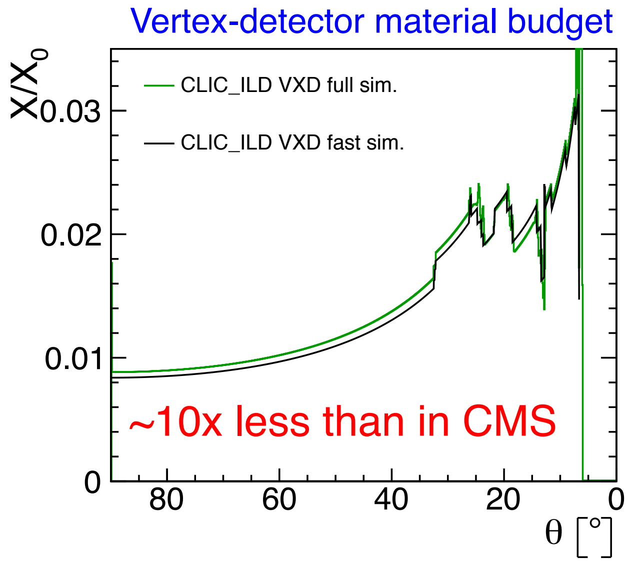
CLIC_ILD vertex region

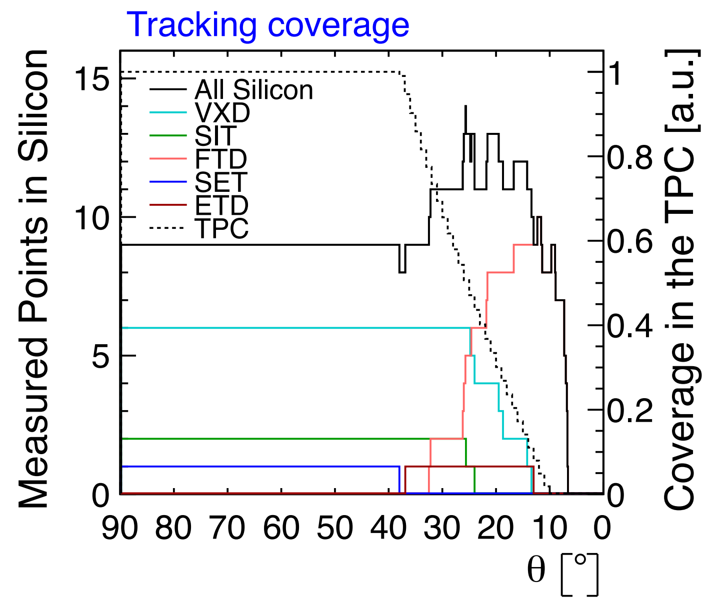


CLIC_SiD

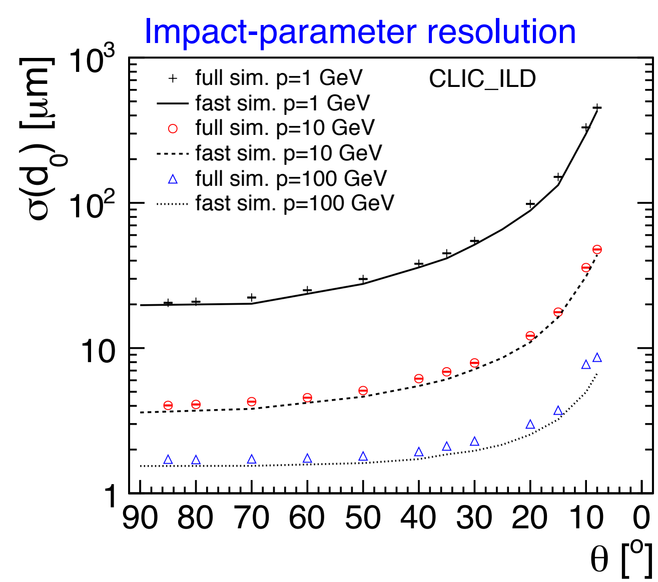


Performance in simulation





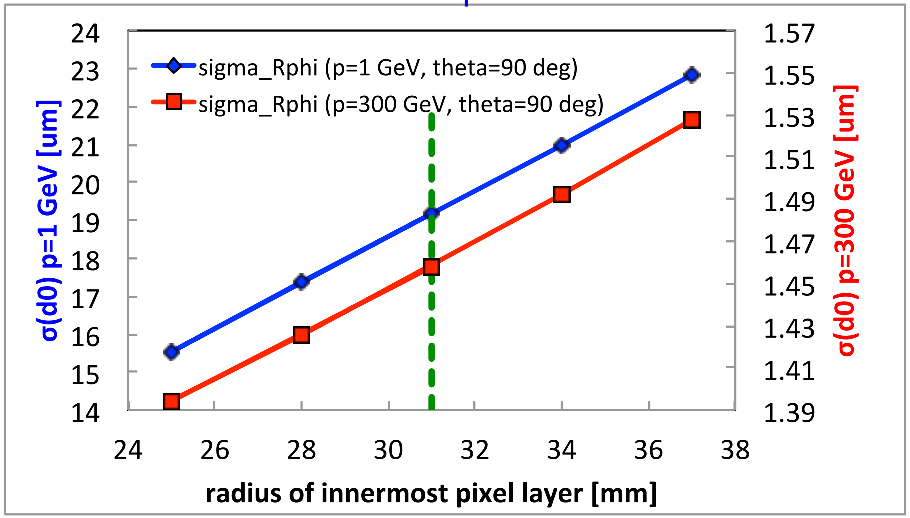
- Baseline physics simulation layouts:
  - very low material budget
  - large coverage
  - excellent performance in simulation
- Engineering studies add realism:
  - increased material budget
  - slightly reduced coverage
- Ongoing studies: assess impact of detector design on performance and develop realistic simulation models
  - parametric fast-simulation studies
  - flavor-tagging performance studies
  - impact on physics performance



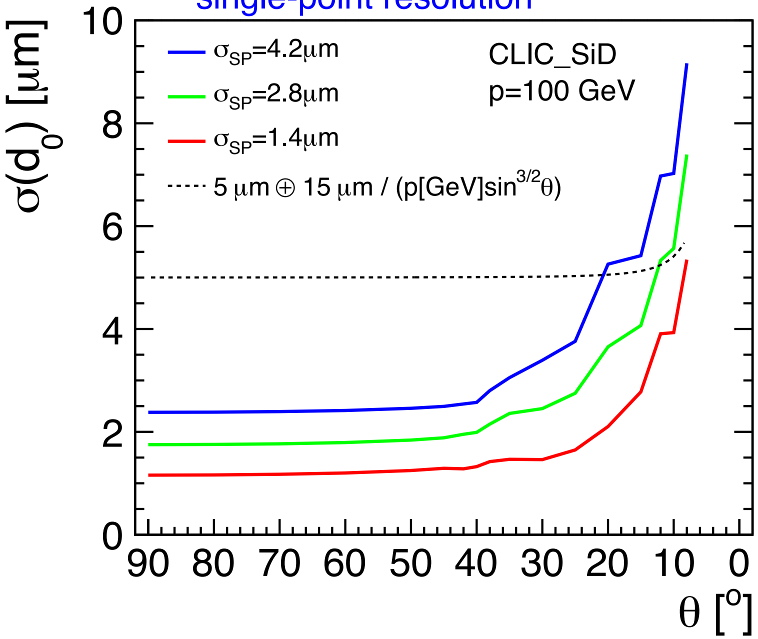
Parametric fast-simulation studies

- Parametric fast-simulation studies
- Main benchmark: transverse impact-parameter resolution σ(d0), closely linked to flavor-tagging perform.
- Assess influence of detector geometry and technology on σ(d0):
  - various detector layouts
  - different single-point resolutions
  - changes in material budget

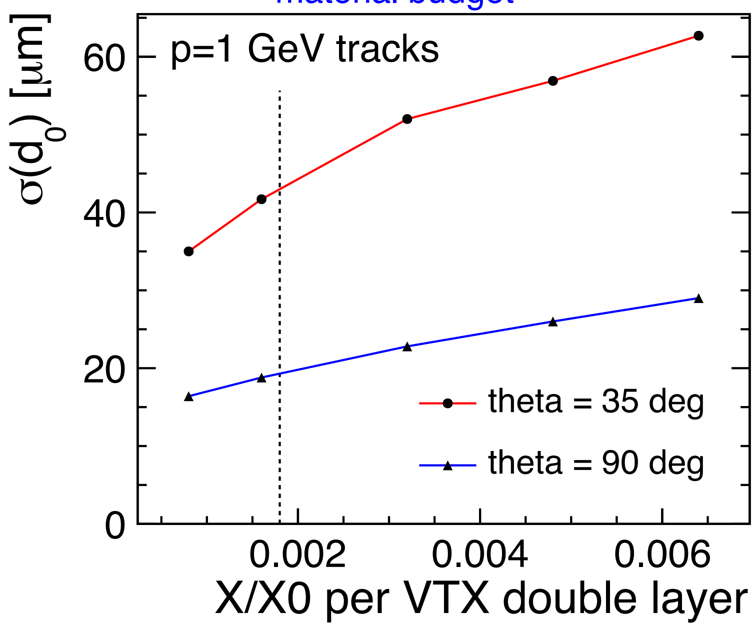
Distance to interaction point



single-point resolution



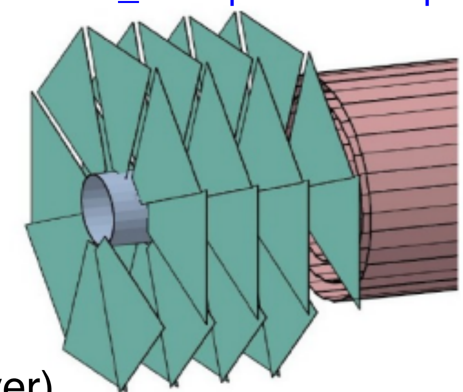
material budget



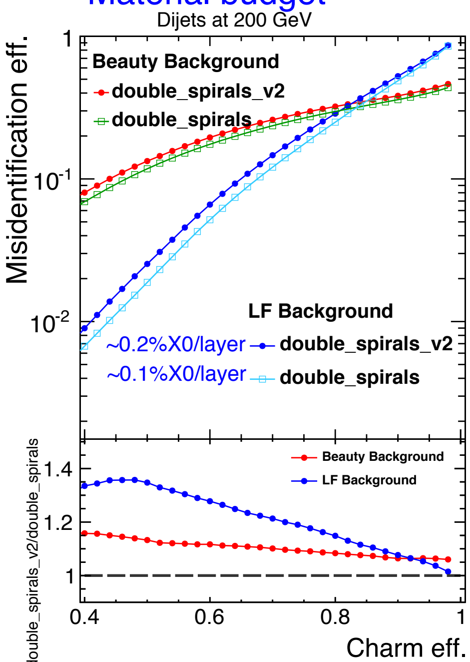
Flavor-tagging performance

- Use b- and c-tagging performance as benchmark for detector designs
- Technically challenging full-simulation study (multivariate analysis)
- Results for geometries following engineering studies:
  - Geometry with 2x more material in vertex layers
    → 5% - 35% degradation in performance
  - Spiral end-cap geometry (required for air-flow cooling)
    → few problematic regions with reduced coverage,
    otherwise similar performance as for disk geometry
  - 3 double layers vs. 5 single layers
    → small improvement for lower-energy jets (less material per layer)

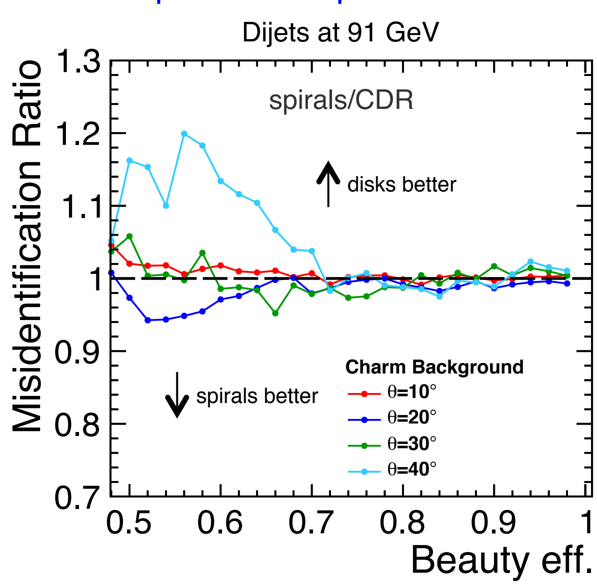
CLIC_SiD spiral end-cap



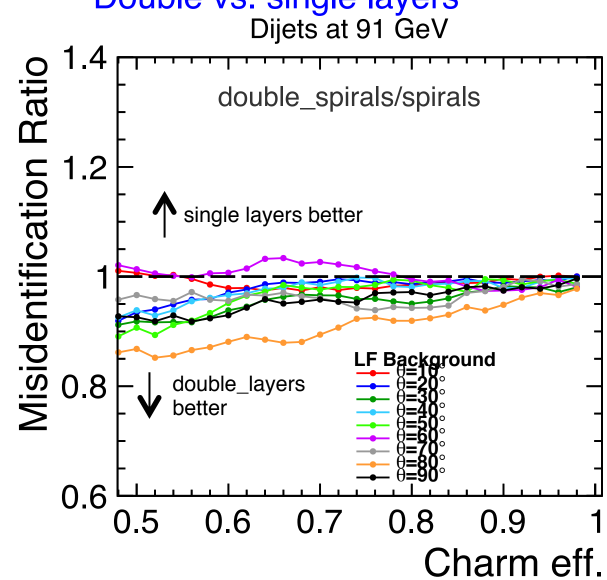
Material budget



Spiral end-caps vs. disks



Double vs. single layers



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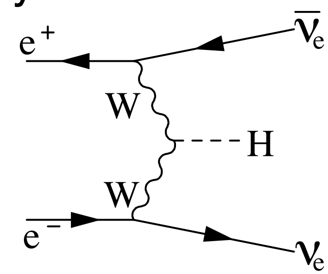
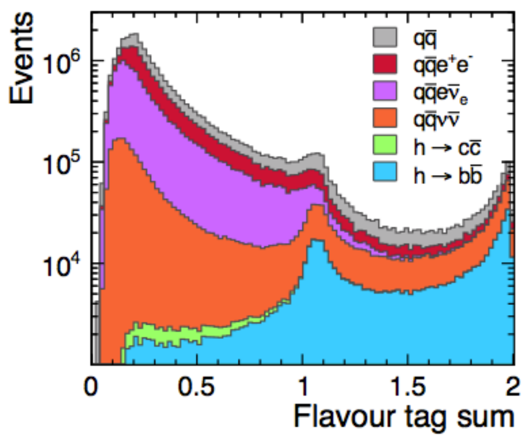
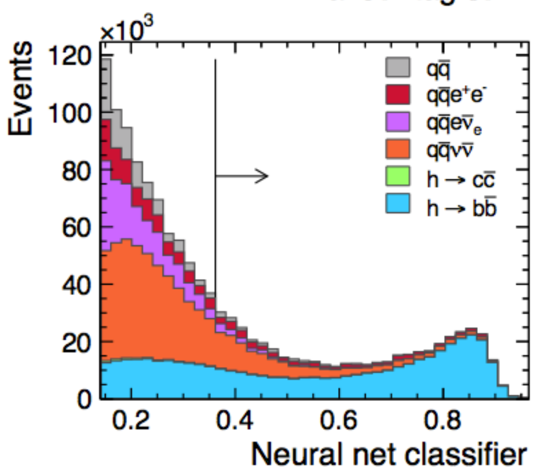
Physics performance

- Ultimate benchmark for vertex-detector: impact on physics analysis results
- Example: achievable precision in $e^+e^- \rightarrow H\nu_e\bar{\nu}_e$, $H \rightarrow b\bar{b}, c\bar{c}$
  - Dominant Higgs-production process at 3 TeV
  - Large backgrounds from light-flavor decays
    → analysis depends strongly on b and c tagging







- Consider ± 20% change in wrong-flavor rejection
- Dominant backgrounds:
  - H→bb: light flavor jets
  - H→cc: light flavor and b-jets
- Impact on achievable statistical precision for cross-section x branching-ratio measurements, for $\sqrt{s}$=3 TeV and L_{int}=2 ab^{-1}:

analysis	stat. uncert. on σxBR	change for ±20% fake rate
H→bb	0.23%	±6-7%
H→cc	3.1%	±15%

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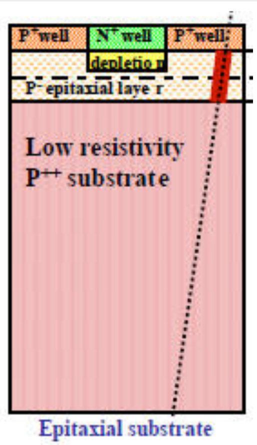
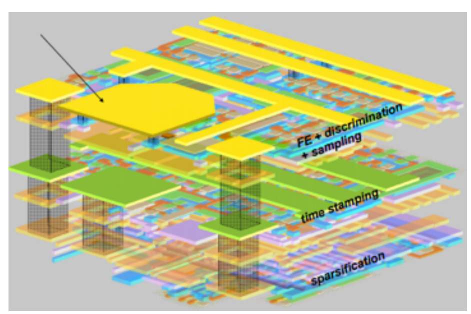
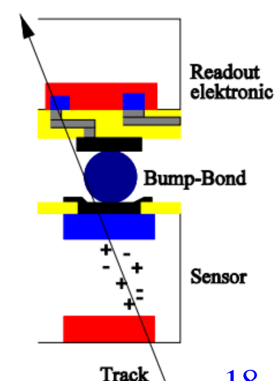
Pixel-detector technologies

	Monolithic	3D-integrated	Hybrid
Examples	FPCCD, MAPS, HV-CMOS	SOI, MIT-LL, Tezzaron, Ziptronix	Timepix3/CLICpix
Technology	Specialised HEP processes, r/o and sensors integrated	Customized niche industry processes, high density interconnects btw. tiers	Industry standard processes for readout; depleted high-res. planar or 3D sensors
Interconnect	Not needed	SLID, Micro bump bonding, Cu pillars	
granularity	down to 5 µm pixel size		~25 µm pixel size
Material budget	~50 µm total thickness achieveable		~50 µm sensor + ~50 µm r/o
Depletion layer	partial	partial or full	full → large+fast signals
timing	Coarse (integrating sensor)	Coarse or fast, depending on implementation	Fast sparsified readout, ~ns time slicing possible
R&D examples	ILC, ALICE, RHIC	ILC, HL-LHC	CLIC, ATLAS-IBL, HL-LHC







Medipix/Timepix hybrid r/o chip family

Chip	Year	CMOS Process	Pitch [μm^2]	Pixel operation modes	r/o mode	Main applications
Timepix	2006	250 nm	55x55	∫TOT or ToA or γ counting	Sequential (full frame)	HEP (TPC)
Medipix3RX	2012	130 nm	55x55	γ counting	Sequential (full frame)	Medical
Timepix3	2013	130 nm	55x55	TOT + ToA, γ counting + ∫TOT	Data driven	HEP, Medical
Smallpix	2014	130 nm	~40x40	TOT + ToA, γ counting + ∫TOT	Sequential (data comp.)	HEP, Medical
CLICpix demonstrator	2013	65 nm	25x25	TOT + ToA	Sequential (data comp.)	Test chip with 64x64 pixel matrix
CLICpix	tbd	65 nm	25x25	TOT + ToA	Sequential (data comp.)	CLIC vertex detector

TOT: Time-Over-Threshold
→ Energy
ToA: Time-of-Arrival
→ Time stamping

- Taking advantage of smaller feature sizes:
  - Increased functionality and/or
  - Reduced pixel size
  - Improved noise performance

Hybrid r/o technology: CLICPix

- **65 nm CMOS hybrid r/o chip**, targeted to CLIC vertex detectors
- based on **Timepix/Medipix** chip family, synergy with HL-LHC pixel r/o projects (**RD 53** collaboration on 65 nm r/o)

- **demonstrator chip** produced with fully functional 64 x 64 pixel matrix
- **25 µm** pixel pitch
- simultaneous **4-bit time (TOA) and energy (TOT)** measurement per pixel

→ front-end **time slicing < 10 ns**

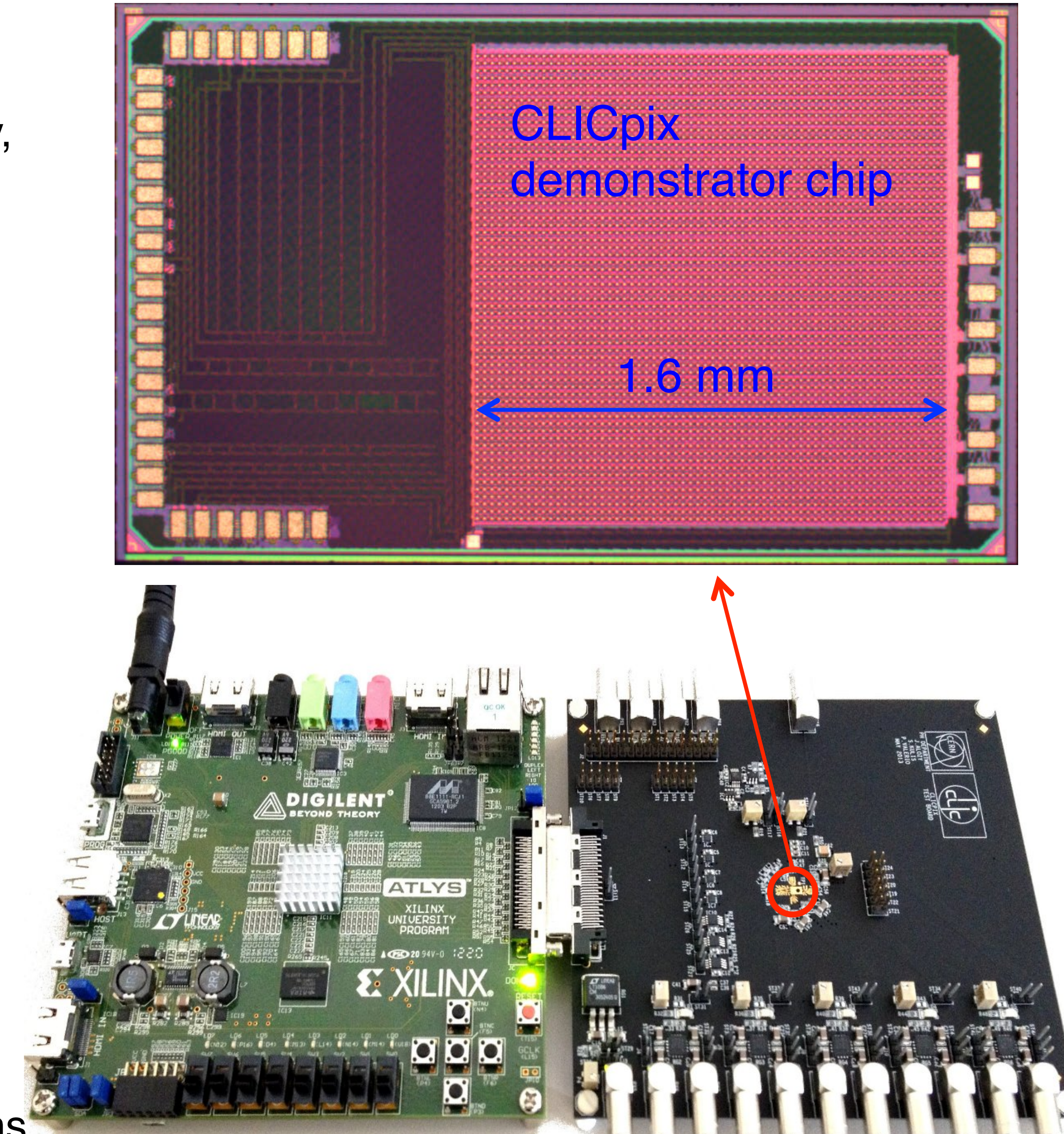
- selectable **compression** logic: pixel, cluster + column-based

→ full chip r/o in less than 800 µs (at 10% occup., 320 MHz r/o clk)

- **power pulsing scheme**

→ $P_{avg} < 50\ mW/cm^2$

- **r/o tests** on prototypes:
  - chip fully functional
  - measurements confirm simulations



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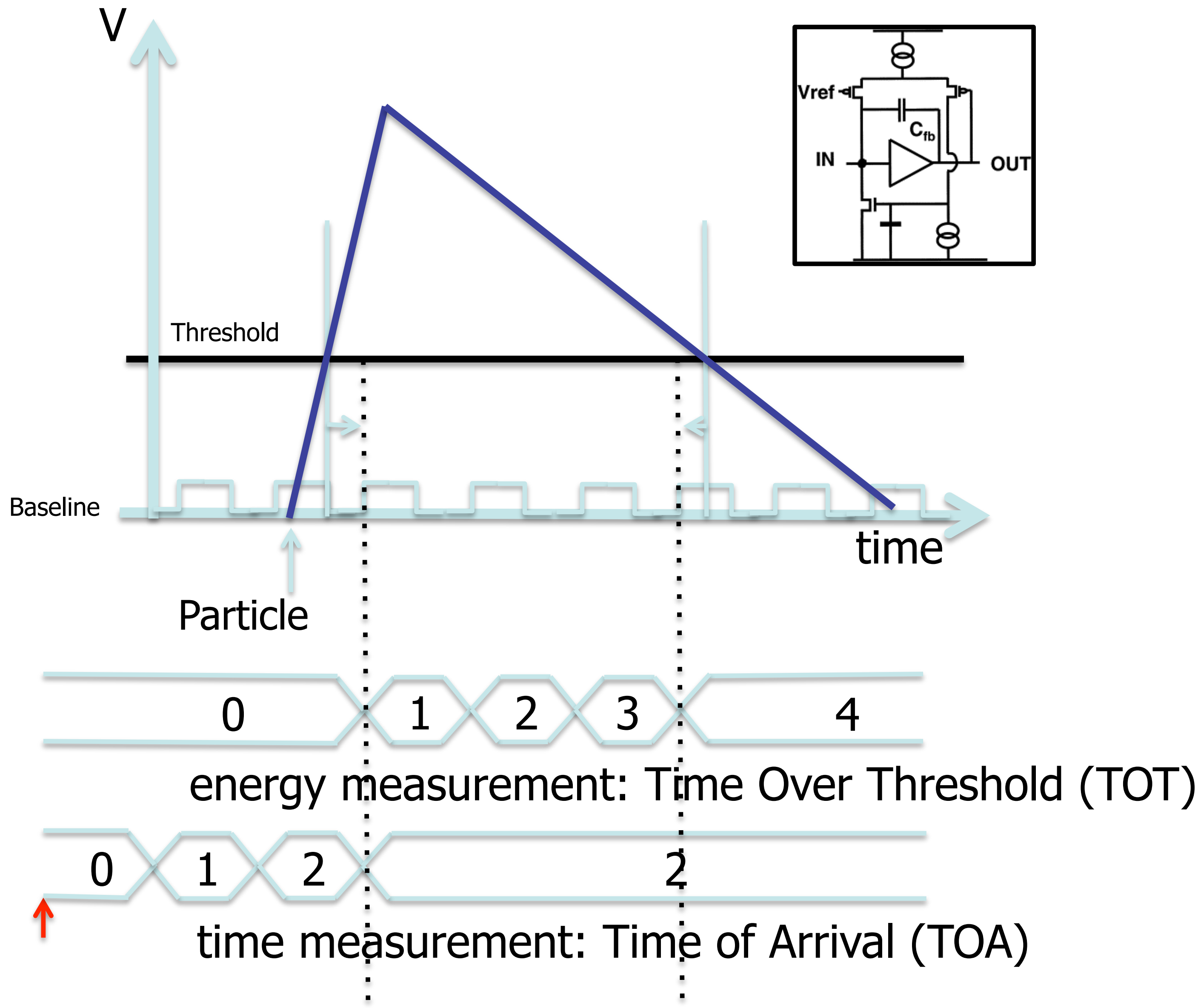
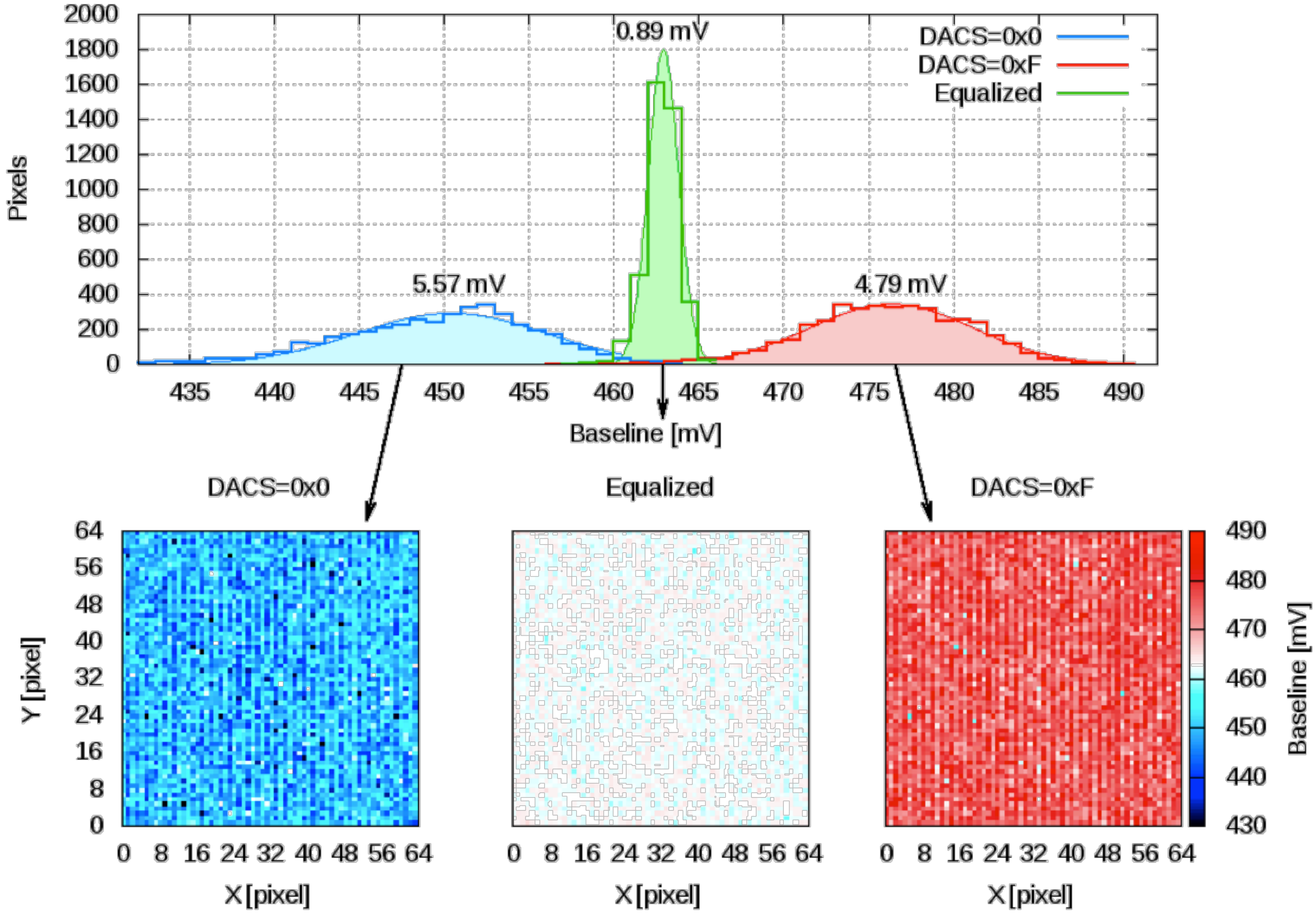
CLICpix: time and energy measurement



CLICpix: baseline equalization



Calibrated spread is 0.89 mV (about 22 e-) across the whole matrix

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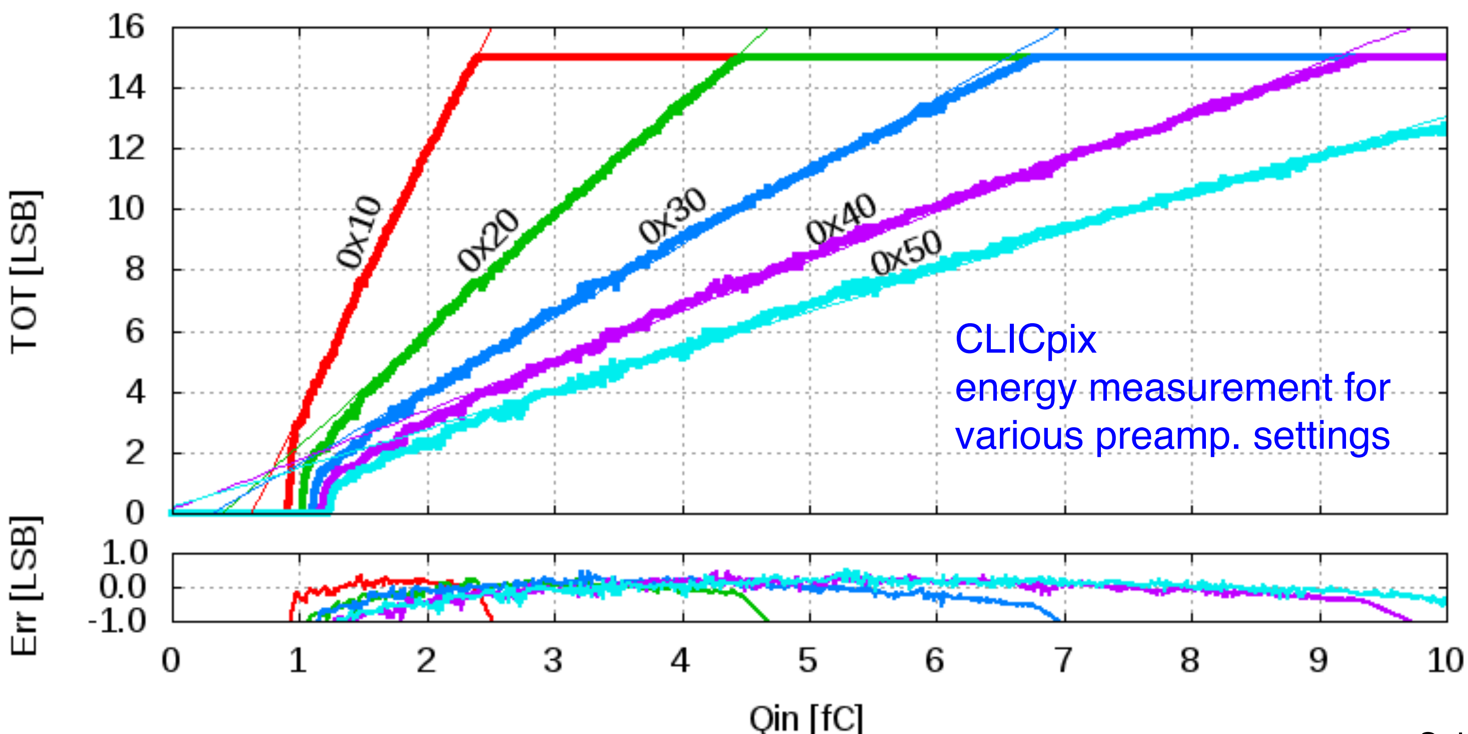
CLICpix: energy measurement

- Measure charge released in each pixel
  → Improve position resolution through interpolation
- Time-Over-Threshold (TOT) measurement (4-bit precision)
- Calibration measurement using external test pulser:



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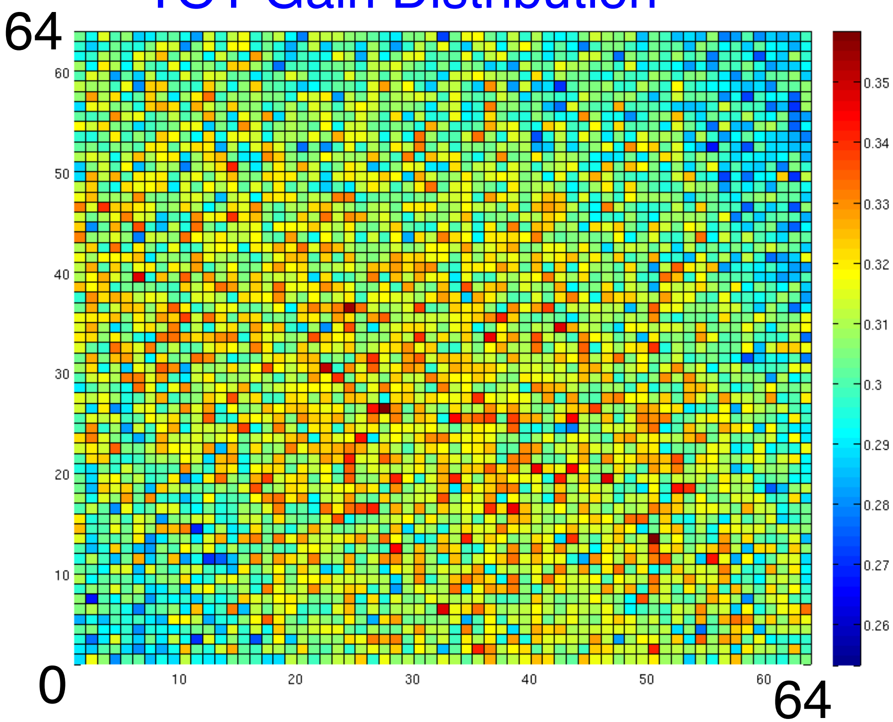
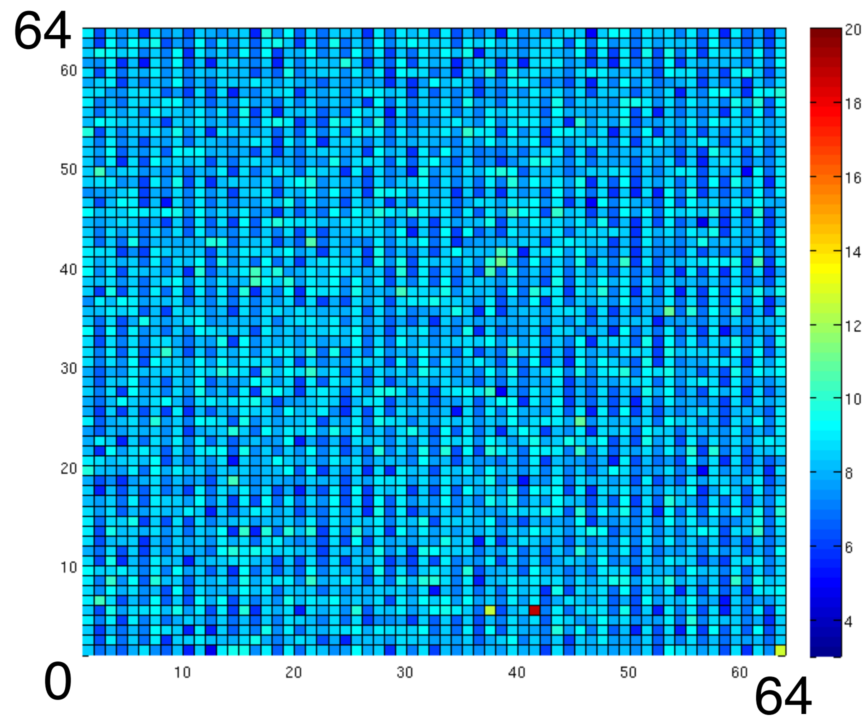
CLICpix: uniformity of gain and noise

TOT Gain Distribution



- Uniform gain across the matrix
- Gain variation ~4.2% r.m.s. (for nominal feedback current)

Equivalent Noise Charge



- Uniform ENC across the matrix
- Mean ENC ~55 e^- (without sensor)

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CLICpix: summary

Parameter	Unit	Simulation	Measurement
Rise time	[ns]	50	-
TOA accuracy	[ns]	<10	<10
Gain	[mV/ke$^-$]	44	40 *)
Dynamic range	[ke$^-$]	44 (configurable)	40 *) (configurable)
INL (TOT)	[LSB]	<0.5	<0.5
ENC (w/o sensor)	[e$^-$]	~60	~55 *)
DC spread σ (uncalibrated)	[e$^-$]	160	128 *)
DC spread σ (calibrated)	[e$^-$]	24	22 *)
Power consumption	[μW/pixel]	6.5	7

*) results obtained with electrical test pulses

- good agreement between simulations and measurements
- power pulsing works according to specifications (>10x reduction for power-off state)
- programmable power on/off times, front-end wake up within ~15 μs
- Radiation test ongoing (up to 1 GRad TID)

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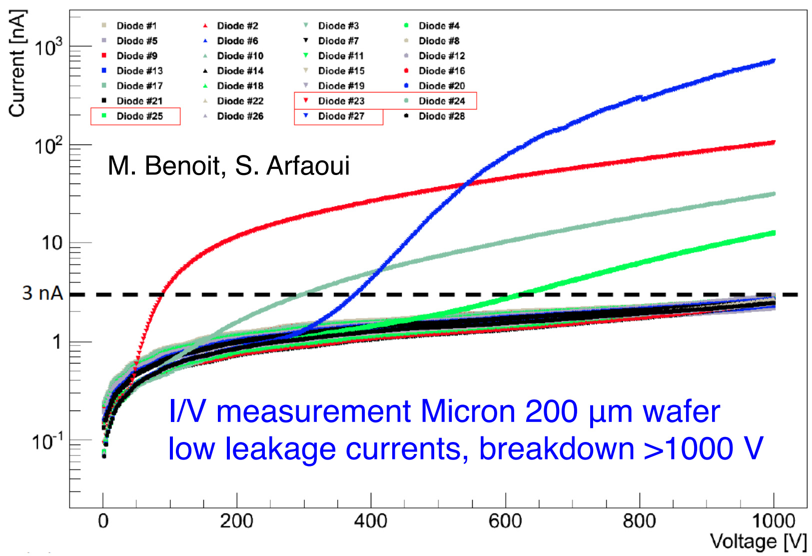
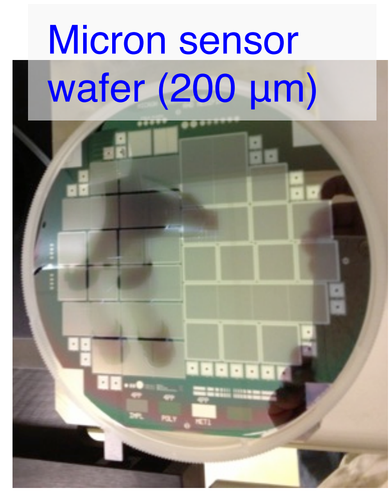
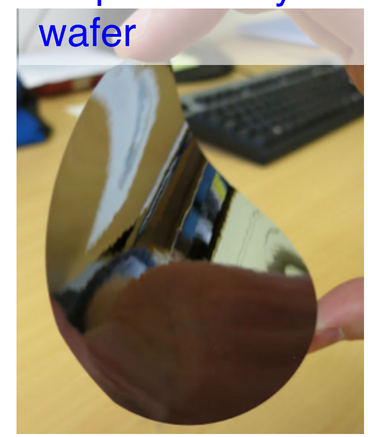
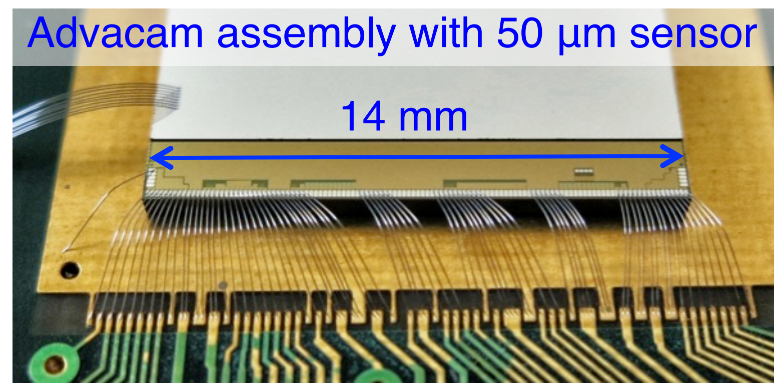
Thin-sensors

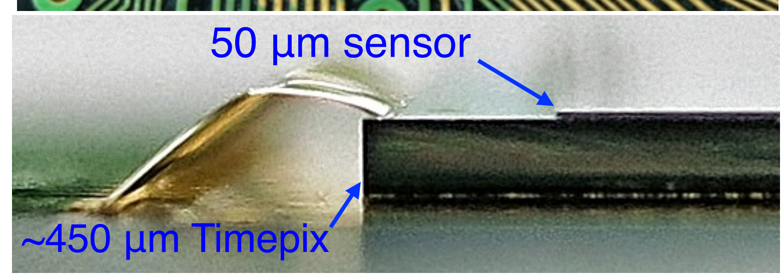
- Micron (UK) + IZM (DE) and VTT/Advacam (FI) Timepix planar sensor assemblies with 55 µm pitch
  - Test feasibility of ultra-thin sensors and assemblies
  - Assemblies delivered: 50-200 µm sensor thickness, 100-450 µm ASIC thickness
  - Test beams at DESY in 2013
  - Sensor calibration (non-linear TOT response)
- sensors matching 25 µm^2 CLICpix footprint → 2014
- ultimate goal: 50 µm thick sensors + 50 µm thick ASICs





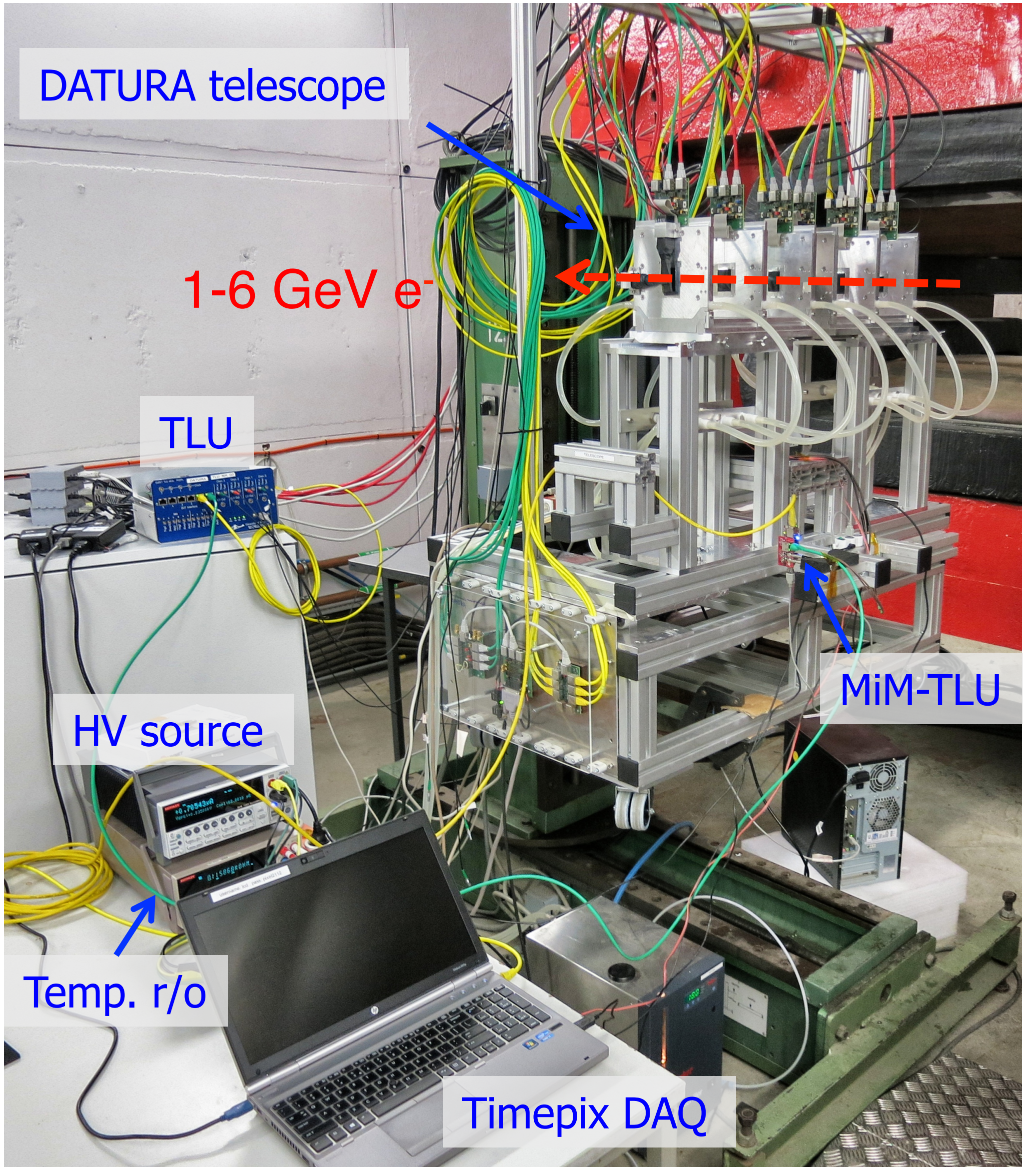


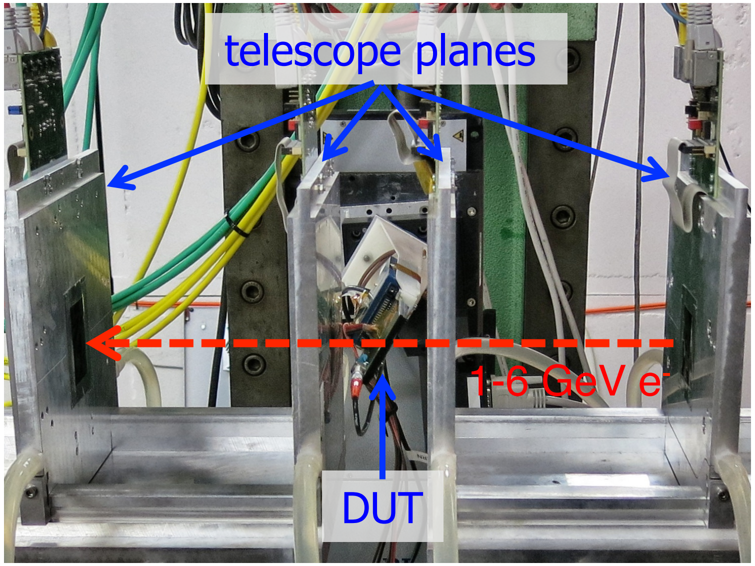


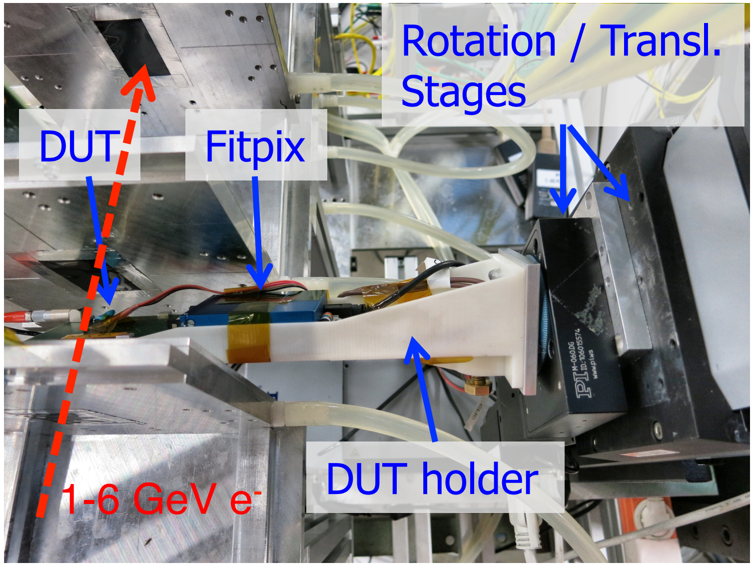


Alternative sensor concepts:
- Low-Gain Avalanche Detectors (LGAD) with charge multiplication
→ thin sensors with large and fast signals (RD50 project with CNM)
- HVCMOS CCPD with capacitive coupling
→ no more bump bonding necessary

Test beam setup at DESY

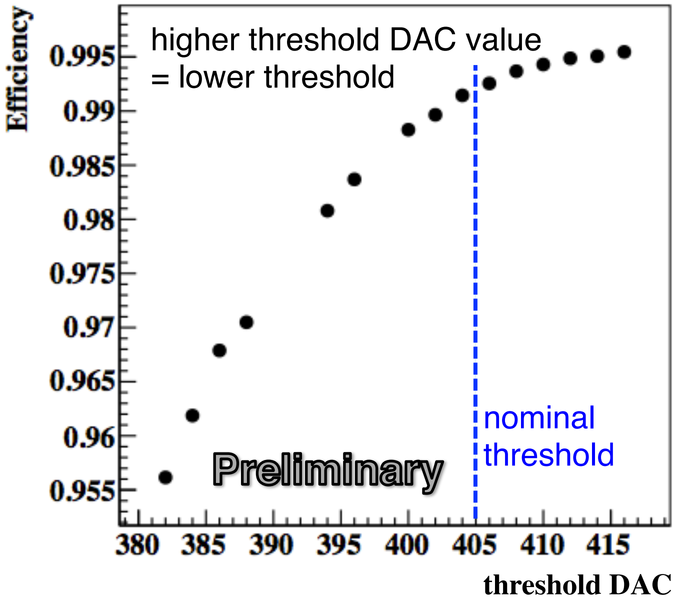






Thin-sensor assemblies in test beam

Threshold scan Advacam 50 μm active edge

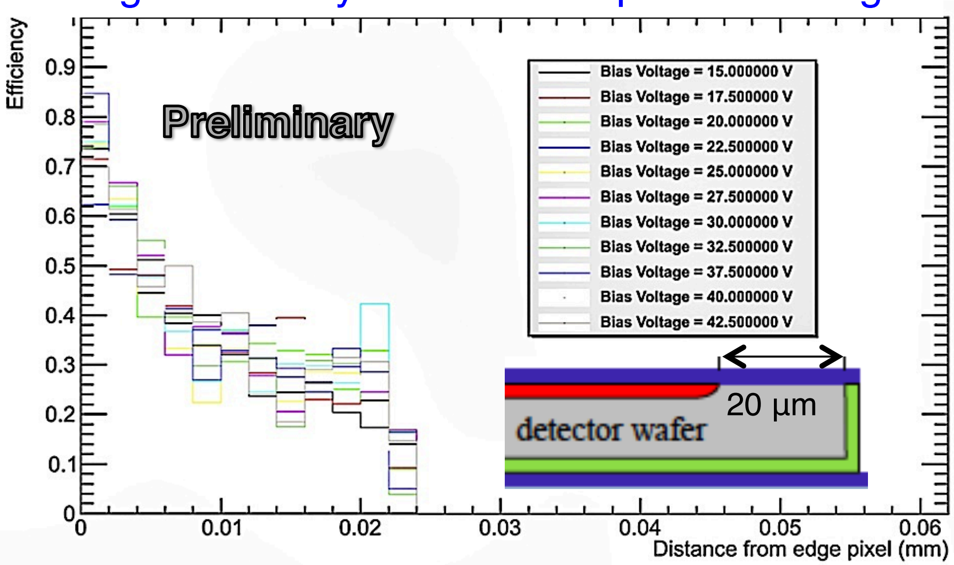


Measurements in DESY II 5.5 GeV e^- beam using DATURA Telescope

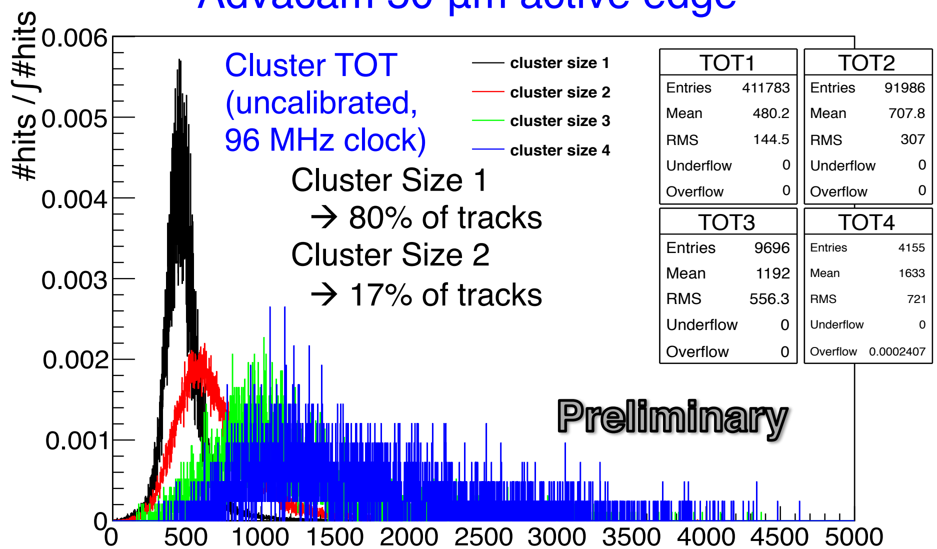
- Assemblies with Advacam p-in-n sensors,
- 50 μm thick, 55 μm pitch
- 20 μm or 50 μm active edges
- Bonded to 450 μm Timepix r/o chip
- Overall Efficiency > 99% (no fiducial cuts)
- Efficiency extends beyond last pixel row

M. Benoit, S. Redford, et al.

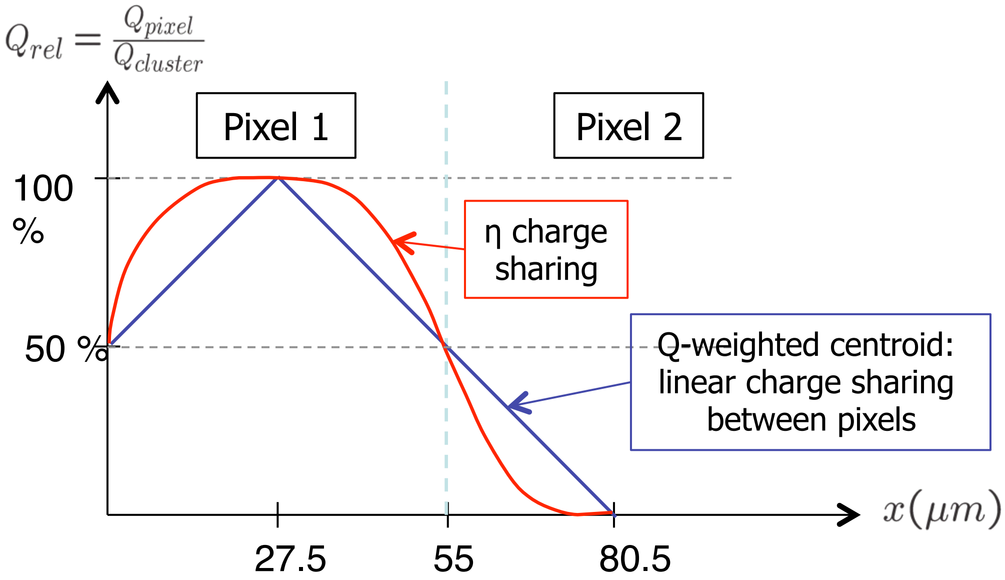
Edge efficiency Advacam 20 μm active edge



Advacam 50 μm active edge



Charge sharing



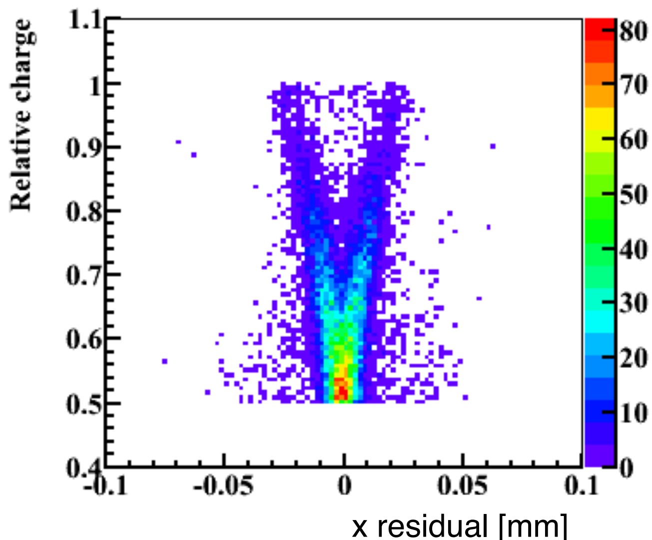
- Non linear charge sharing between pixels, parameterized by η function:

$$\eta(x) = Q_{cluster} \times \frac{erf(\frac{x}{\sigma})+1}{2} \qquad if\ x < pitchX/2$$

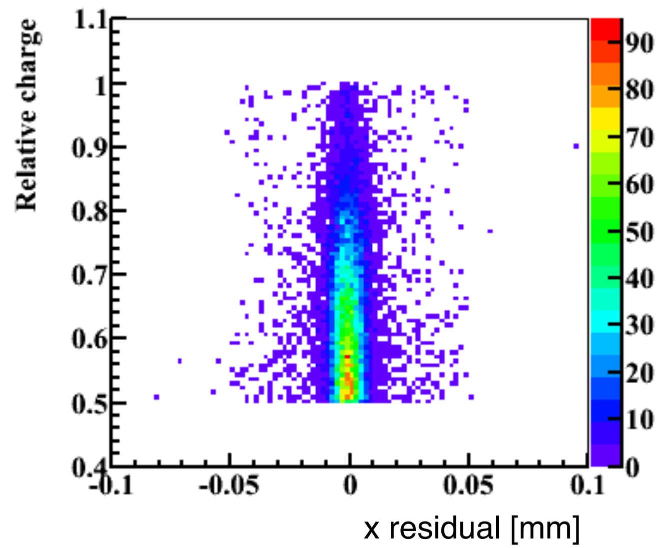
$$\eta(x) = Q_{cluster} \times \frac{erf(\frac{pitchX-x}{\sigma})+1}{2} \qquad if\ x > pitchX/2$$

- Single parameter σ describing diffusion of charge cloud in electric field
- Obtain σ from minimization of position resolution

Linear interpolation



η correction



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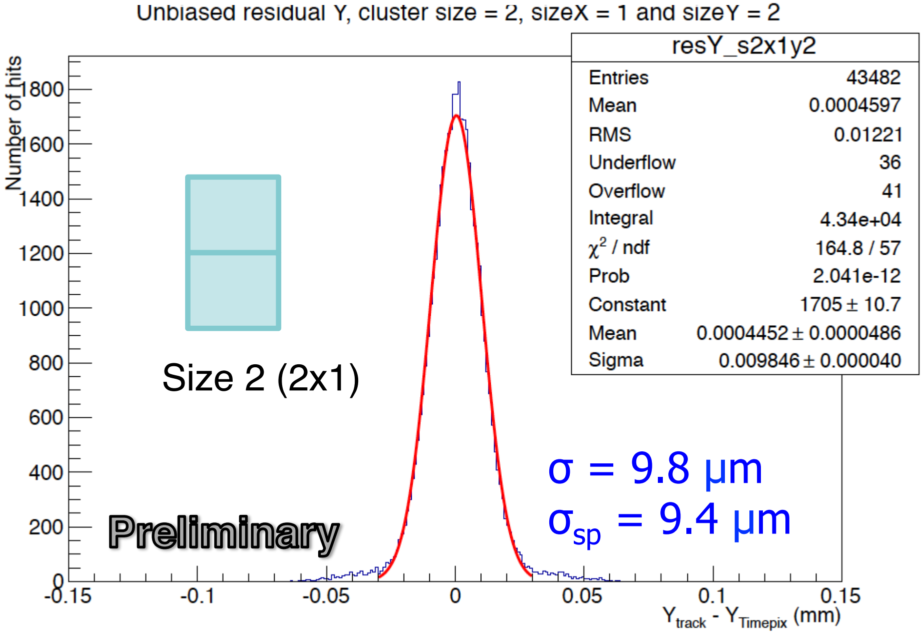
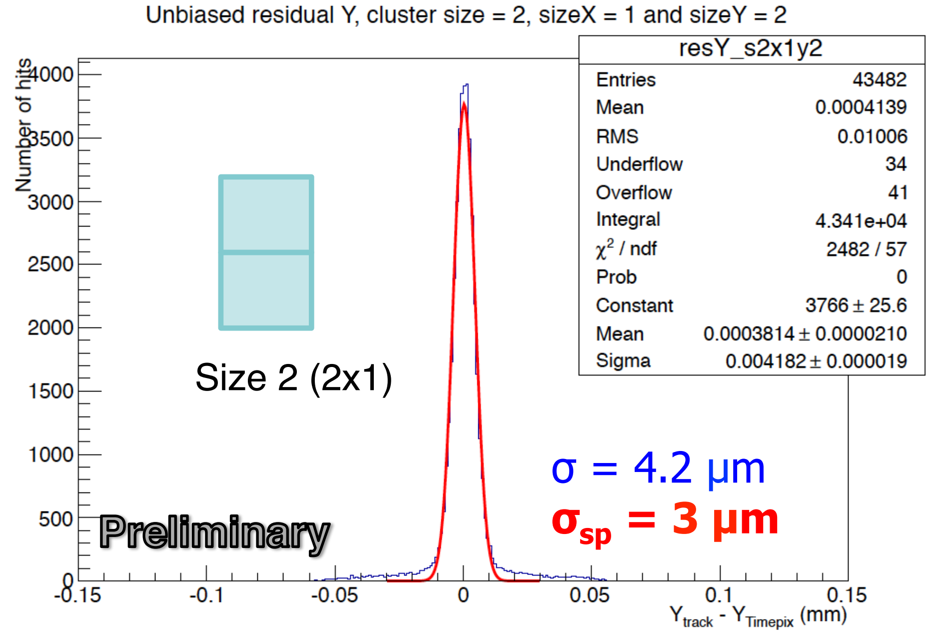
Resolution with eta correction

- Comparison linear interpolation / η correction for 2-hit clusters (17% of all tracks):
  σ_{SP}~9 µm for linear interpolation
  σ_{SP}~3 µm with η correction
- Note: selection bias of 2-hit clusters not unfolded

Linear interpolation



η correction



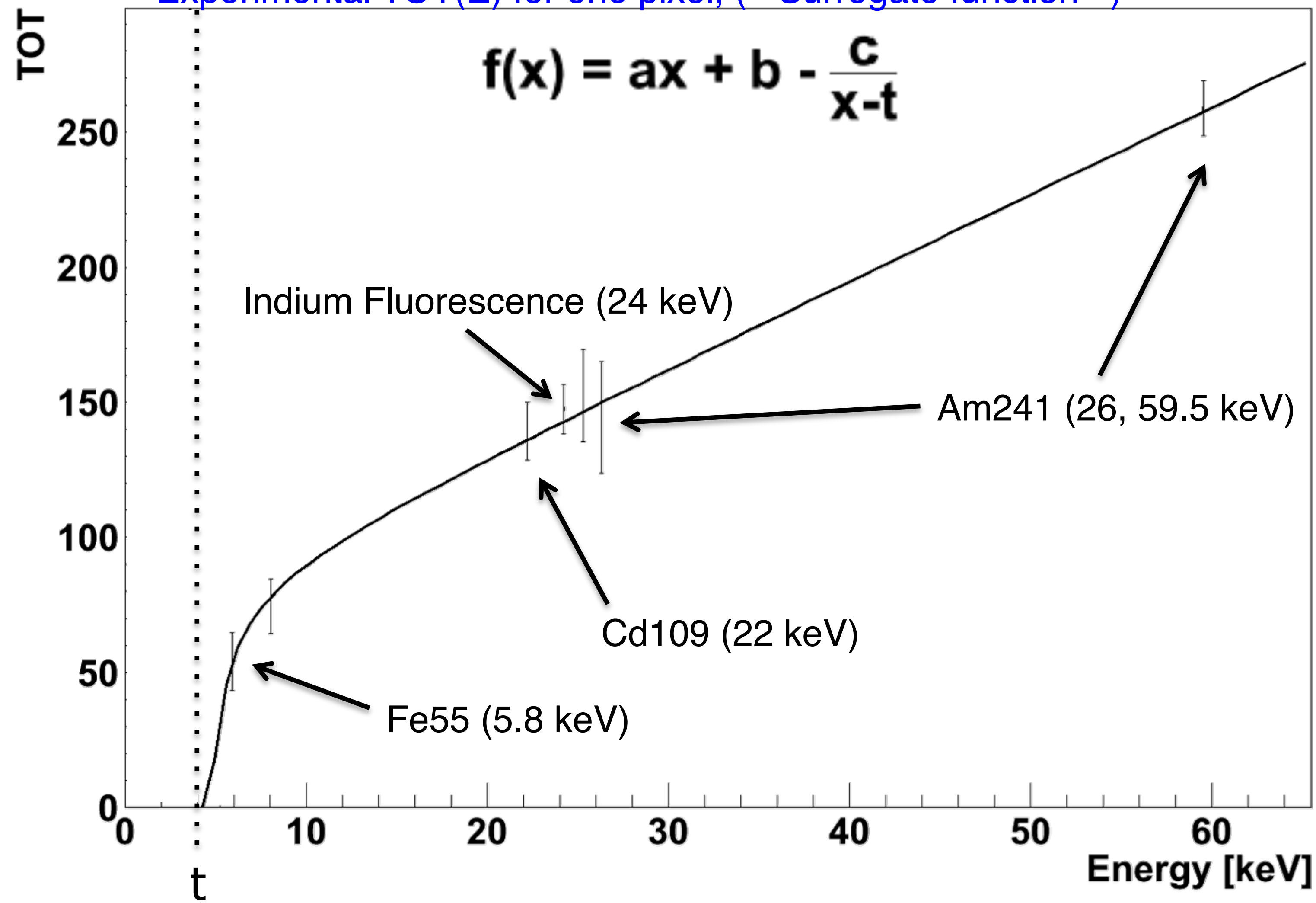
M. Benoit et al.

Timepix calibration

- Calibration of non-linear Timepix energy response with radioactive sources + fluorescence
- Parameterization with 4 parameters per pixel

→ Improves accuracy of position determination with charge-weighting methods

Experimental TOT(E) for one pixel, (« Surrogate function »)



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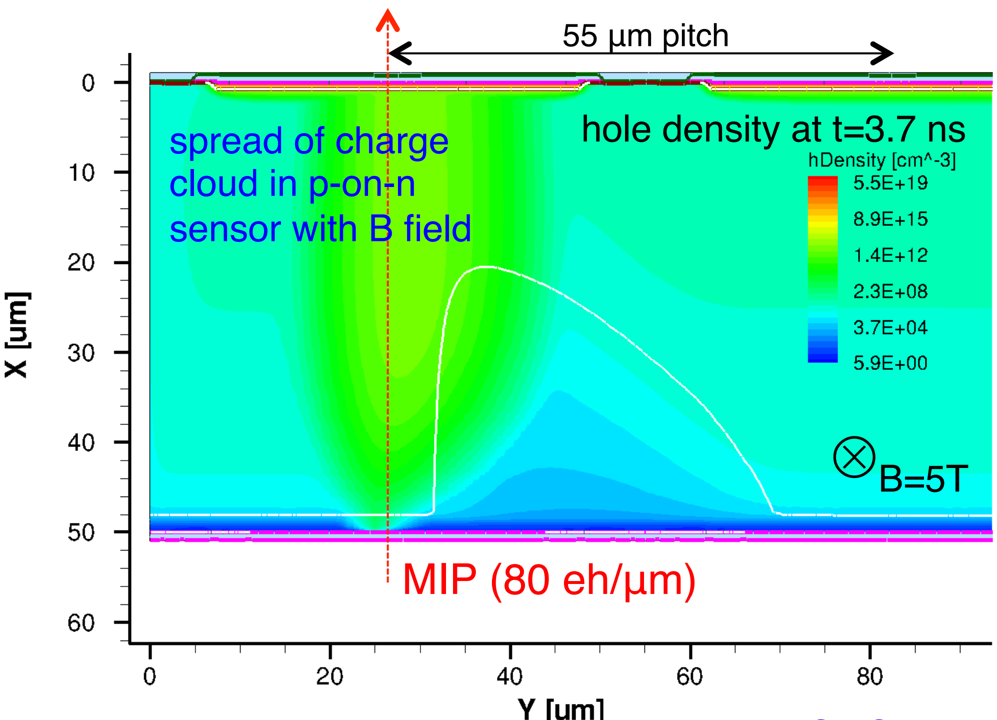
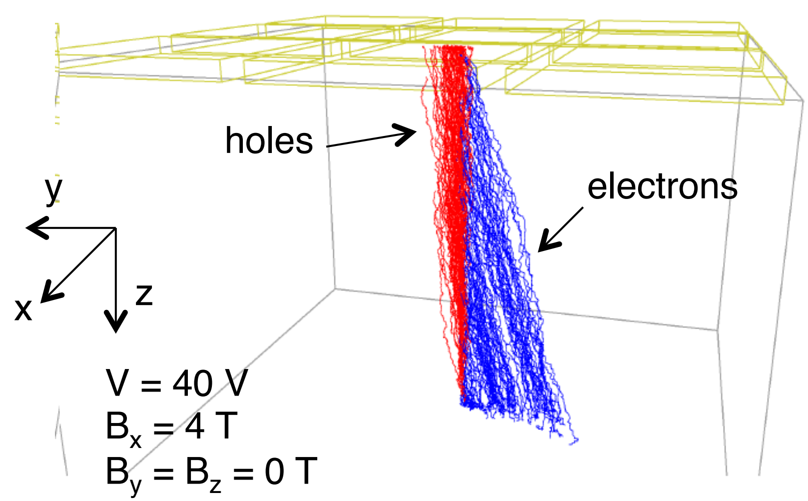
Simulations

- TCAD and MC simulations of charge propagation in silicon sensors
  - → effect of sensor layout and material
  - → effect of E and B fields (Lorentz angle)
  - → comparison with lab and test-beam measurements
  - → tuning of digitization models for full-detector simulation
- ALLPix general purpose pixel detector simulation and digitisation framework
  - → used for simulation of test-beam and lab measurements
  - → One-day tutorial at CERN on January 24th



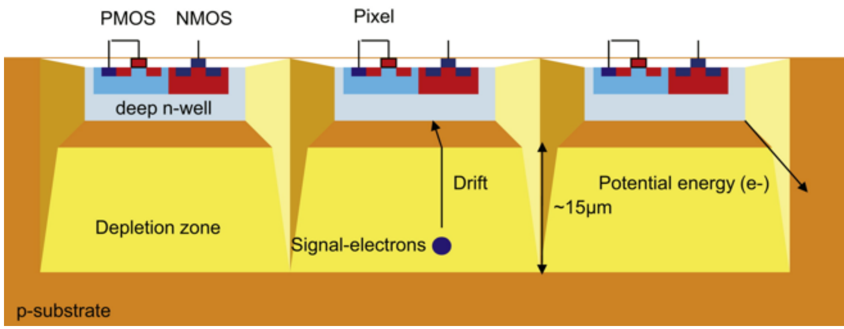
Carrier drift in 50 µm thick fully depleted sensor:



Integrated / hybrid technology: HV-CMOS

HV-CMOS MAPS:

- 180 nm High-Voltage CMOS process:
  Vbias~100 V → depletion layer ~10-20 µm
- integrated sensors with fast signal collection
- baseline technology for Mu3e at PSI

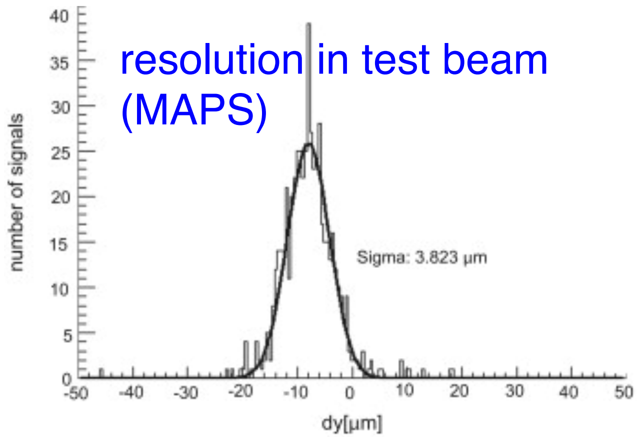


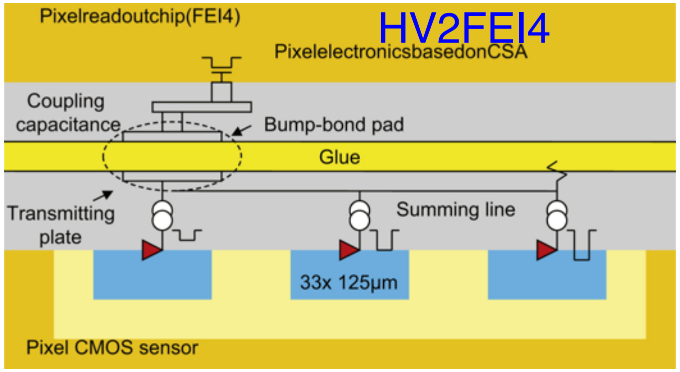
Hybrid option:

Capacitive Coupled Pixel Detector (CCPD)

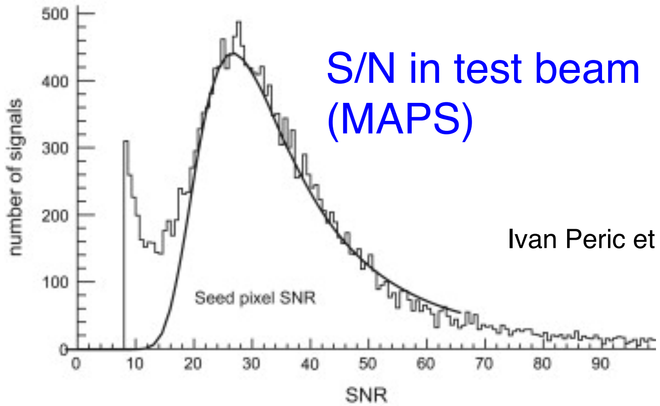
- HV-CMOS chip as integrated sensor+amplifier
- capacitive coupling from amplifier output to r/o chip through layer of glue → no bump bonding!
- test chip for ATLAS FEI4 and Timepix produced
- proof of principle measurements

resolution in test beam (MAPS)





S/N in test beam (MAPS)



Ivan Peric et al.

Heidelberg, CERN, CPPM, Bonn, Geneva, Glasgow

HV-CMOS ATLAS/CLICpix prototype CCPDV3

New HVCMOS prototype, to test capacitive coupling with CLICpix demonstrator

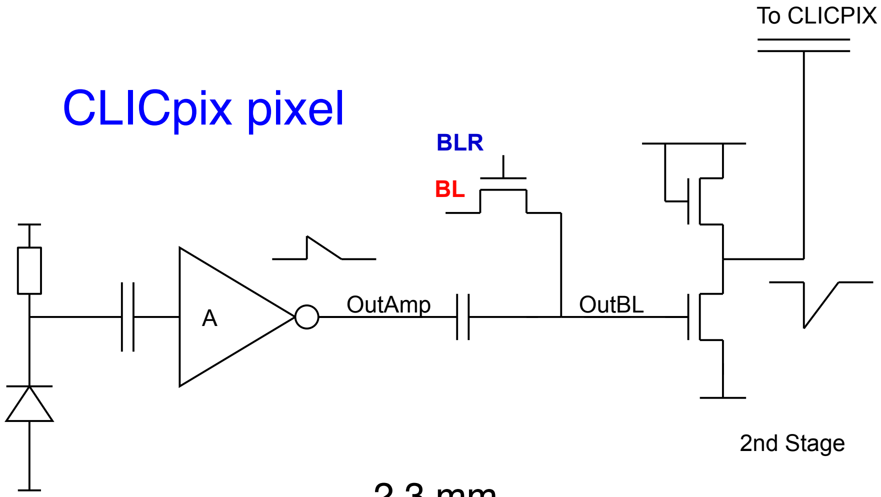
6.4 mm^2 split in ATLAS FEI4 + CLICpix parts

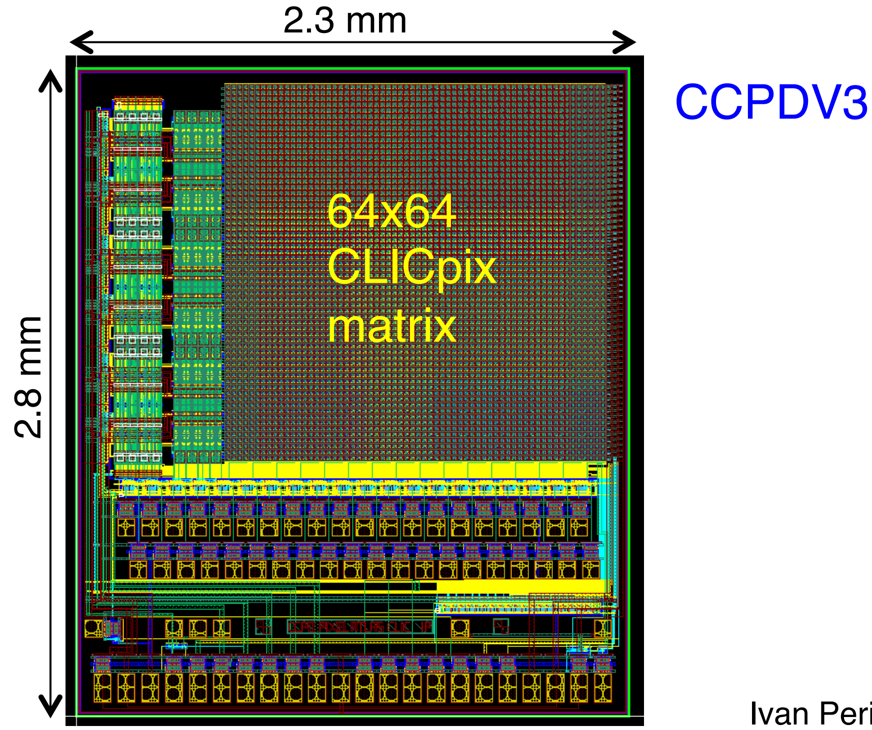
Includes 64x64 CLICpix matrix with 25 µm pitch

2-stage amplifier

AMS H18 180 nm process

Submission November 2013





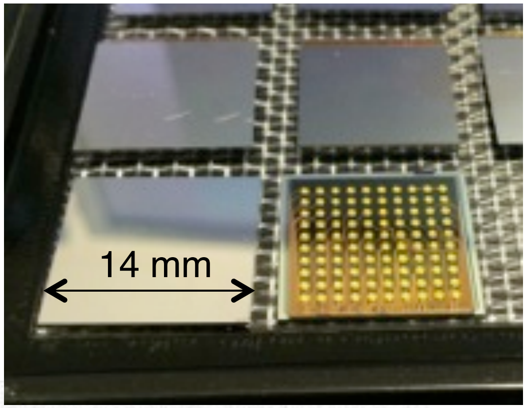
Ivan Peric

Through-Silicon Vias (TSV)

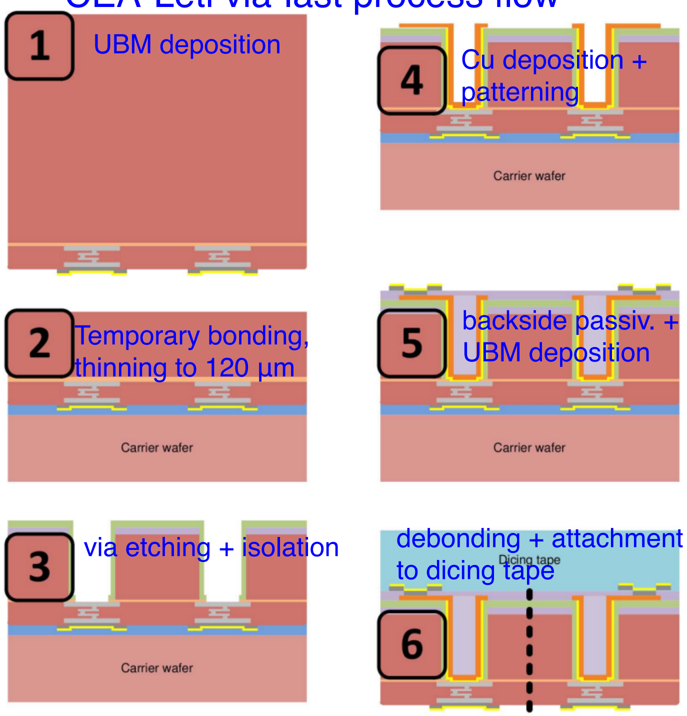
Through Silicon Via (TSV): vertical electrical connection passing through Si wafer
→ eliminates need for wirebonds
→ 4-side buttable chips
→ increased reliability, reduced material budget

Example: Medipix TSV project (ALICE, CLIC, ACEOLE and AIDA) with CEA-Leti

- 130 nm IBM Medipix(RX) wafers, via-last process
- successful completion of first phase: demonstrate feasibility
- on-going second phase: demonstrate good yield



CEA-Leti via-last process flow



http://iopscience.iop.org/1748-0221/6/11/C11018/pdf/1748-0221_6_11_C11018.pdf

- 240 µm TSV diameter
- wafers thinned to 120 µm
- 5 µm copper layer for TSV

First Medipix3 Image taken with TSV assembly:

Medipix Collaboration + CEA-Leti

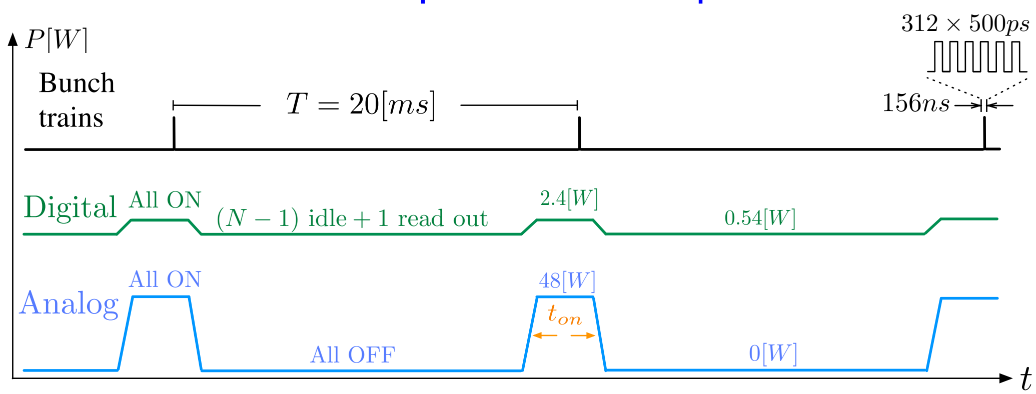
CLICpix power-pulsing + delivery requirements

Small duty cycle of CLIC machine allows for power reduction of readout electronics: turn off front end in gaps between bunch trains

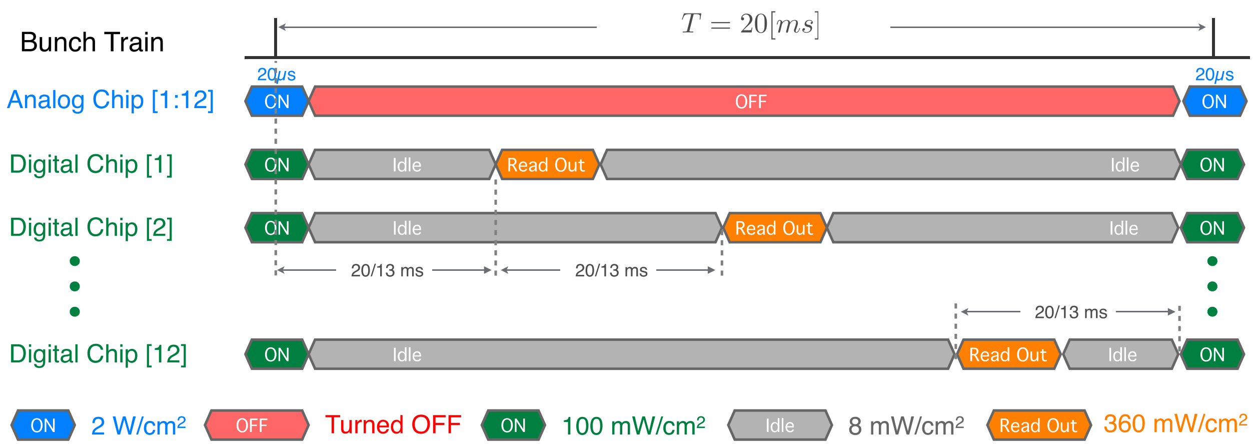
Challenging requirements:

- Power budget **<50 mW/cm²** average (air-flow cooling limit)
- High peak current **> 40A/ladder**
- Different timing analog/digital electronics
- High magnetic field **4-5T**
- Material budget **< 0.1% X_0** for services+supports
- Regulation **< 5% (60 mV)** for analog part

Vertex-detector power consumption



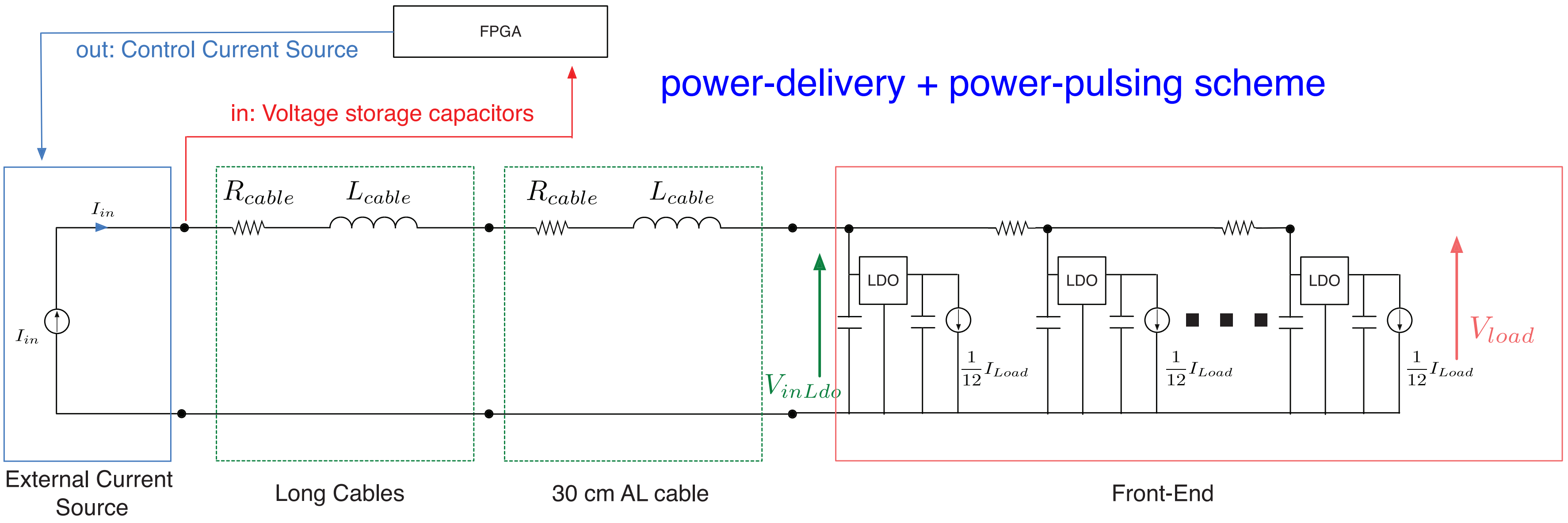
CLICpix powering states



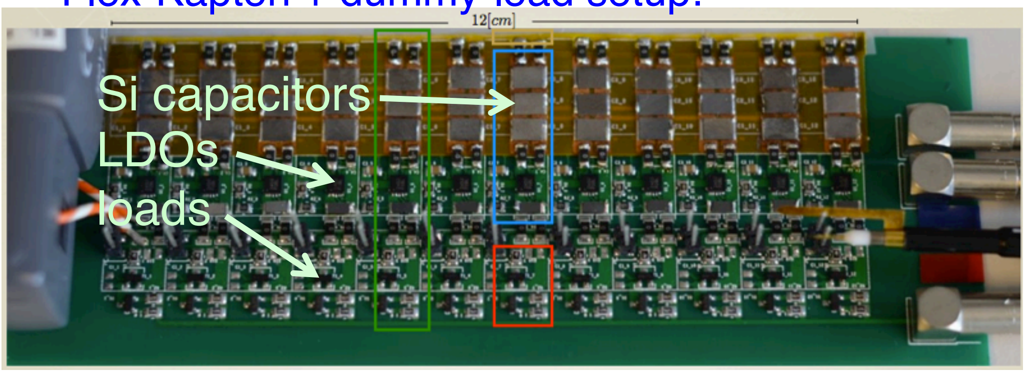
C. Fuentes, X. Llopart, P. Valerio

CLICpix power-pulsing + delivery concept

power-delivery + power-pulsing scheme



Flex-Kapton + dummy-load setup:

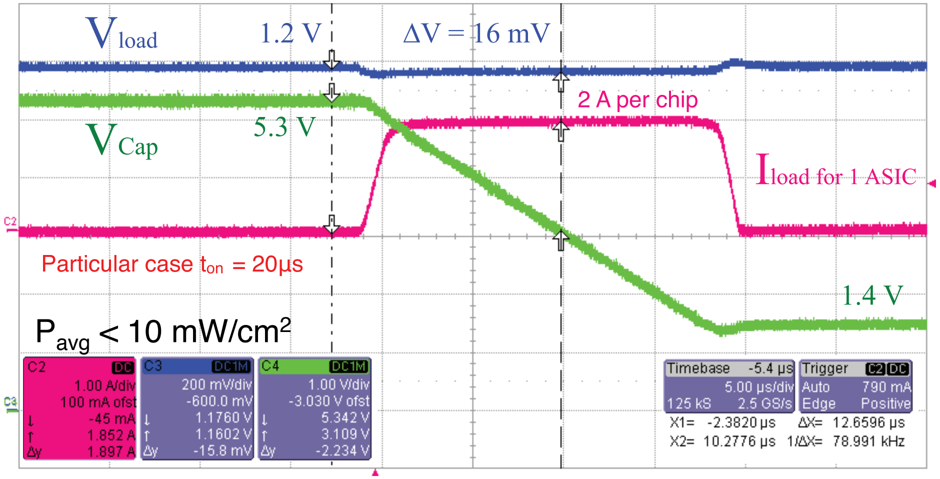


- Power pulsing with local energy storage in Si capacitors and voltage regulation with Low-Dropout Regulators (LDO)
- FPGA-controlled current source provides small continuous current
- Low-mass Al-Kapton cables
- Prototypes for analog + digital powering of CLICpix ladder

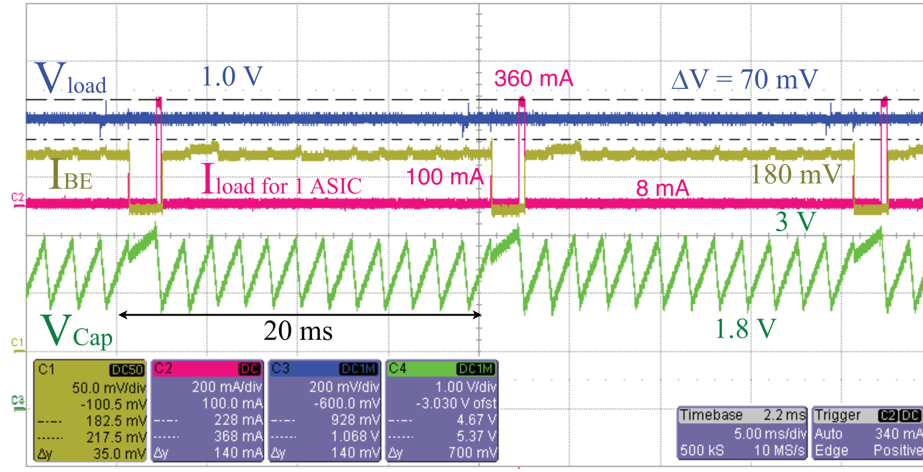
C. Fuentes

CLICpix power-pulsing + delivery results

analog power

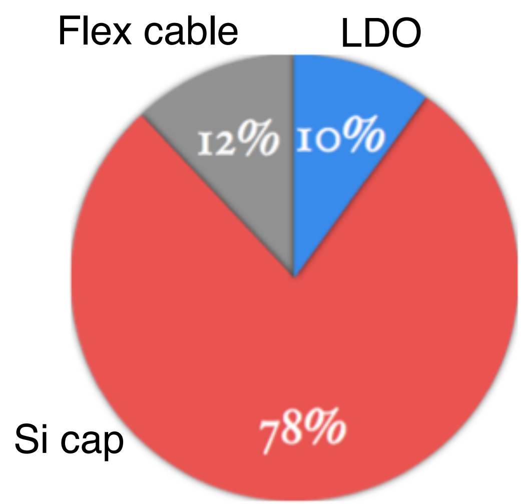


digital power



- Measurements on prototypes for digital and analog powering of ladders:
  - I_{ladder}<300 mA; P<45 mW/cm²
  - Voltage stability:
    ΔV~16 mV (analog), ~70 mV (digital)
  - ~0.1% X_0 material contribution, dominated by Si capacitors
  - Can be reduced to ~0.04% X_0 with evolving Si capacitor technology: 25 µF/cm² → 100 µF/cm²

material budget



C. Fuentes

X/X0~0.104%

Cooling: simulations

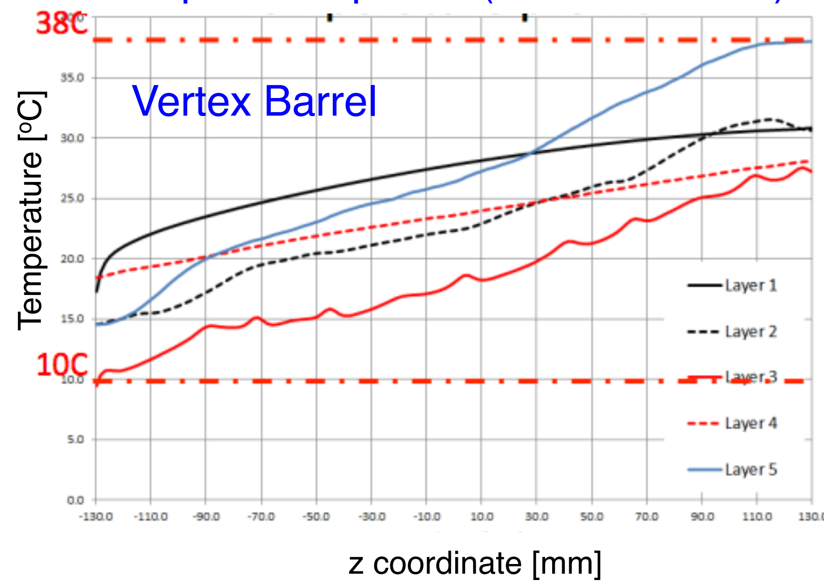
Cooling studies for CLIC vertex detector

- ~500 W power dissipation in CLIC vertex area
- spiral disks allow air flow through detector
- ANSYS Computational Fluid Dynamic (CFD) finite element simulation

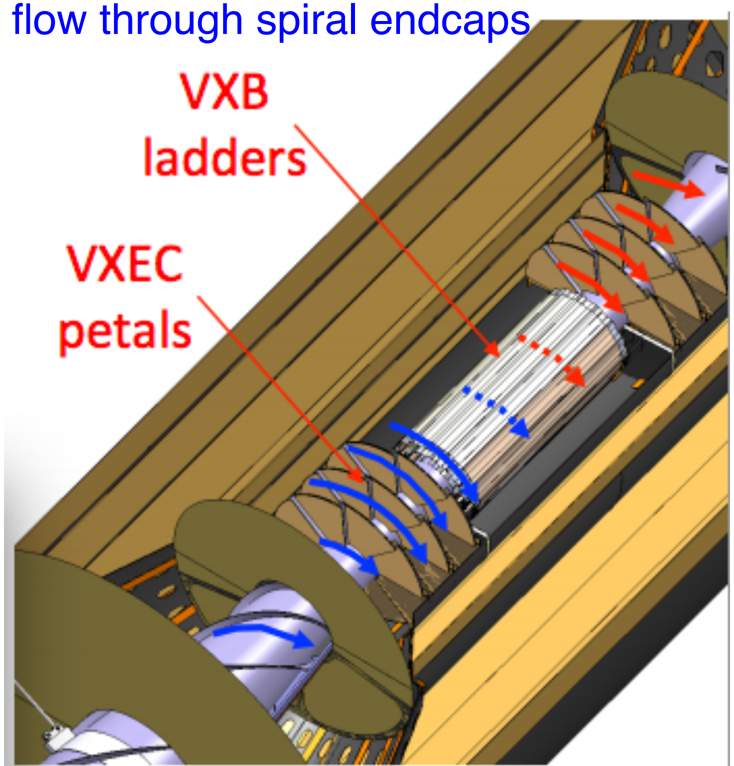
→ air cooling seems feasible

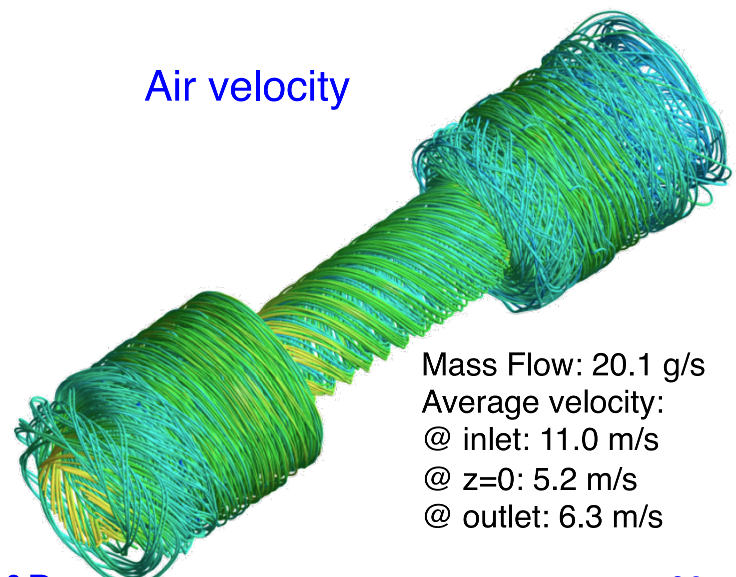
- 5-10 m/s flow velocity, 20 g/s mass flow

Temperature profile (FE simulations)



Air flow through spiral endcaps



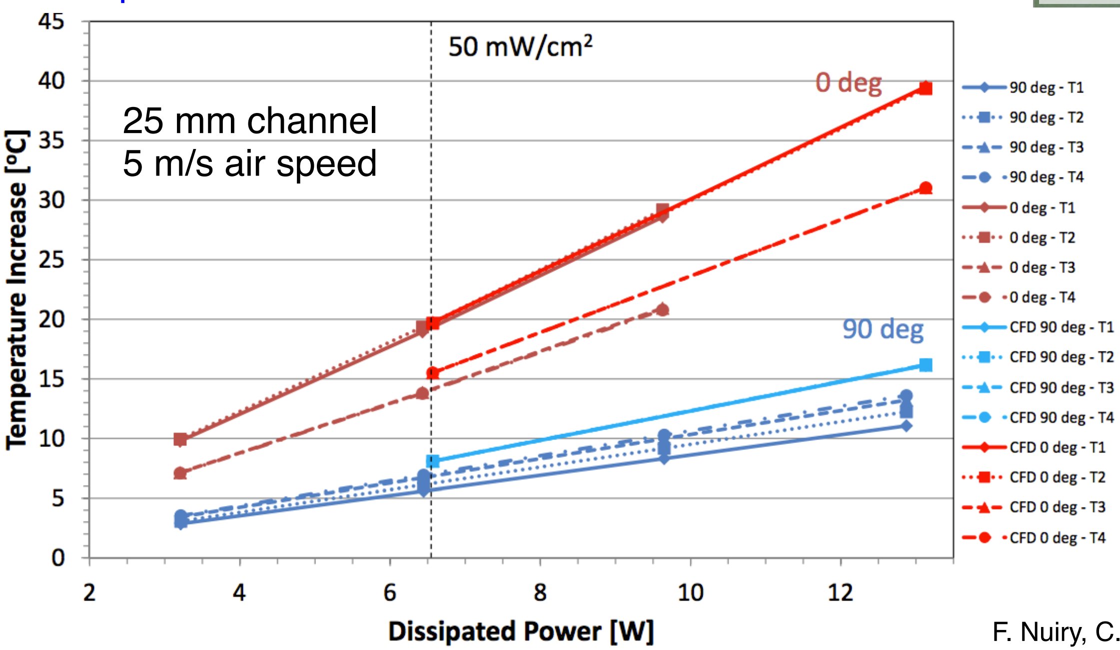


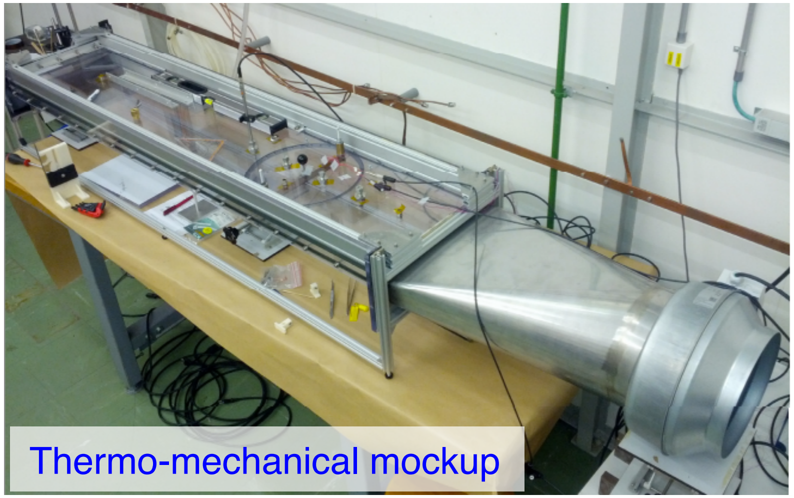
F. Duarte Ramos

Cooling: experimental verification

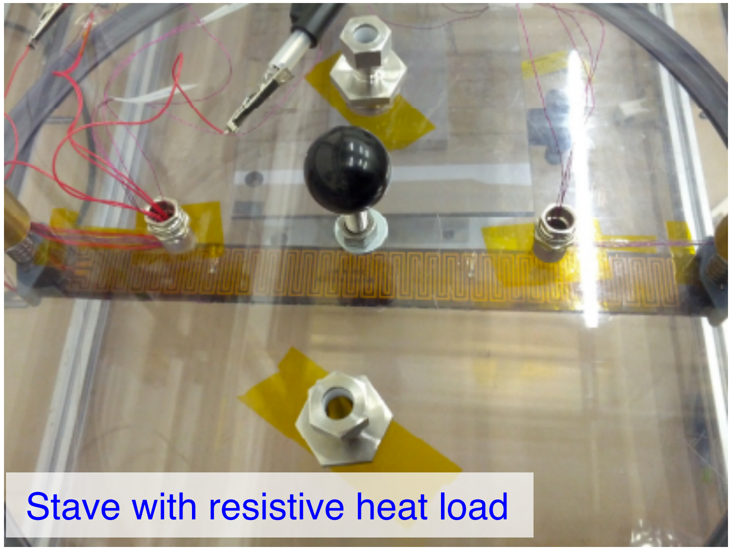
- built mock-up to verify simulations (temperature, vibrations)
- measurements on single stave equipped with resistive heat loads:
  - air flow
  - temperature
  - vibrations (laser sensor)
- comparison with simulation

Temperature increase: measurement + CFD simulation





Thermo-mechanical mockup



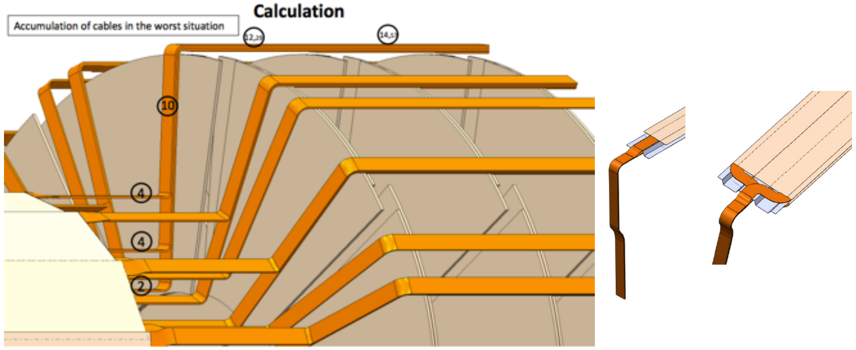
Stave with resistive heat load

F. Nuiry, C. Bault, F. Duarte Ramos, M.-A. Villarejo Bermudez, W. Klempt

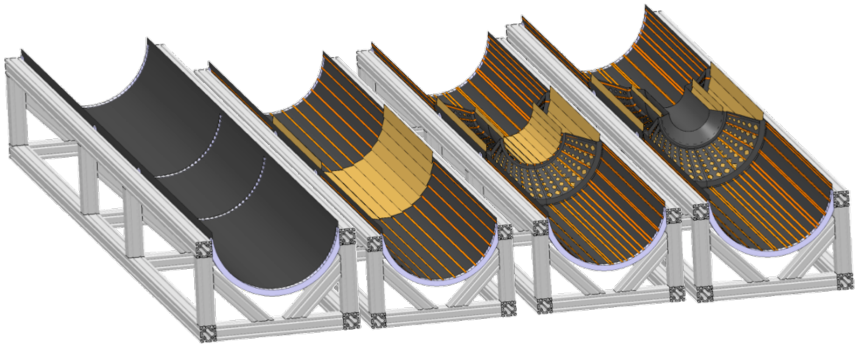
Mechanical integration

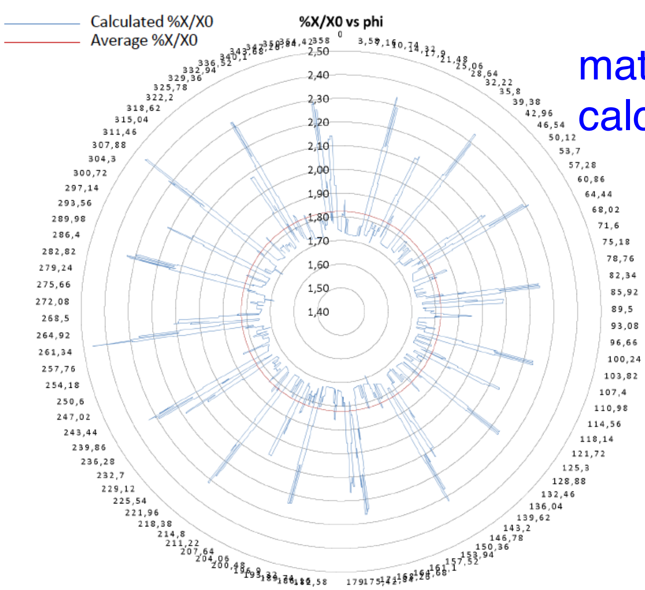
- Detector integration: low-mass supports, services, assembly
- Taking into account constraints from powering and cooling
- Detailed material-budget calculations, comparison with simulation models

vertex-detector services

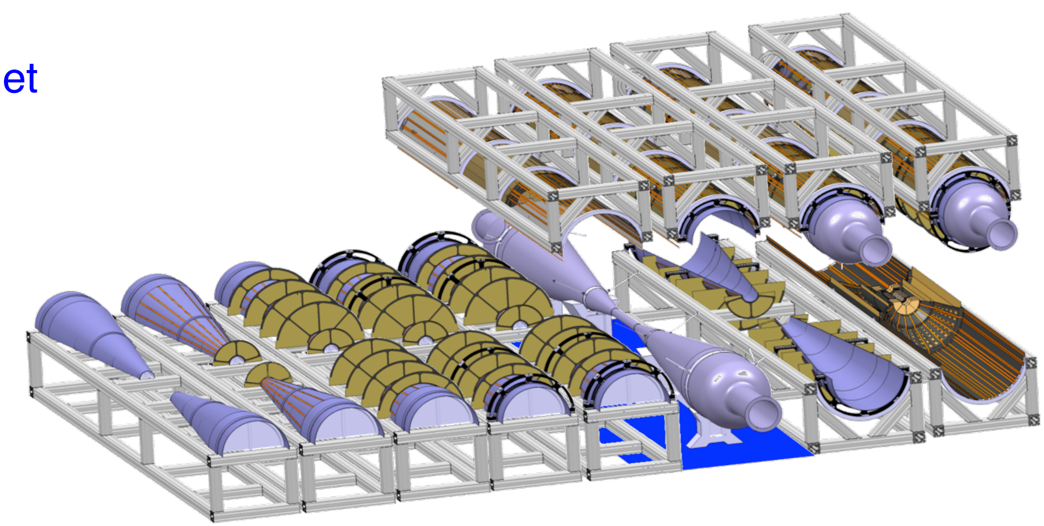


assembly scenario





material-budget calculation



F. Duarte Ramos, M.-A. Villarejo Bermudez

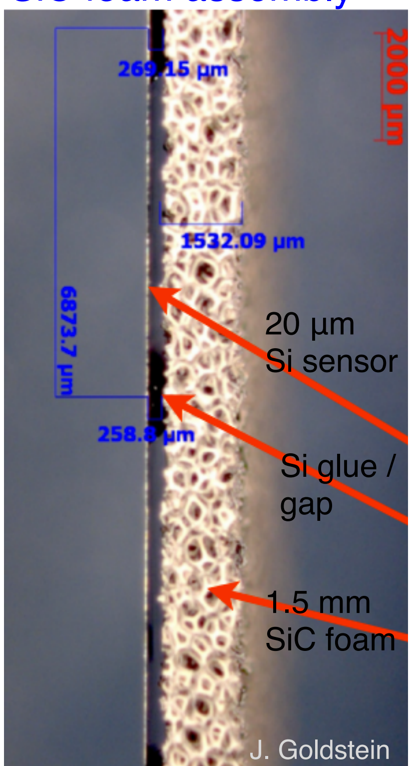
Low-mass supports

- Aim for only ~0.1% X0 per layer for powering + supports

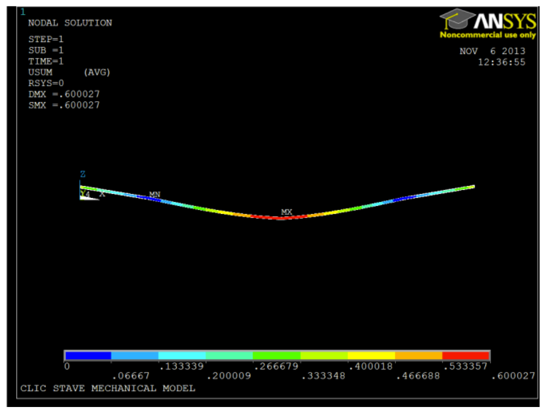
→ ~0.05% X0 for supports

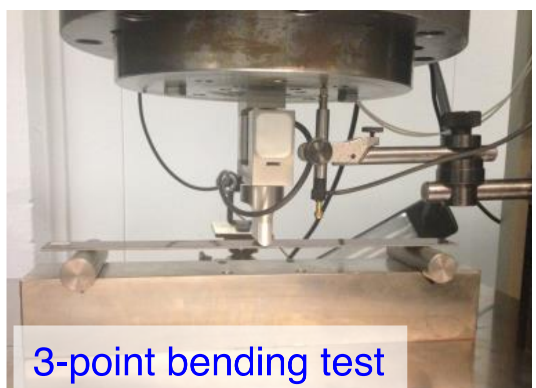
- Evaluating various designs and materials based on:
    - Carbon-Fiber-Reinforced Polymers (CFRP)
    - Silicon-Carbide (SiC) foams
- Bending stiffness validated with calculations, finite-element simulations and measurements

SiC foam assembly

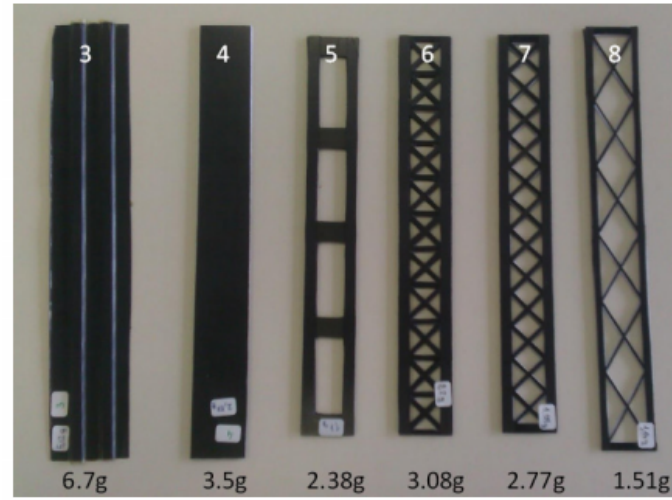


ANSYS FE simulation for CFRP

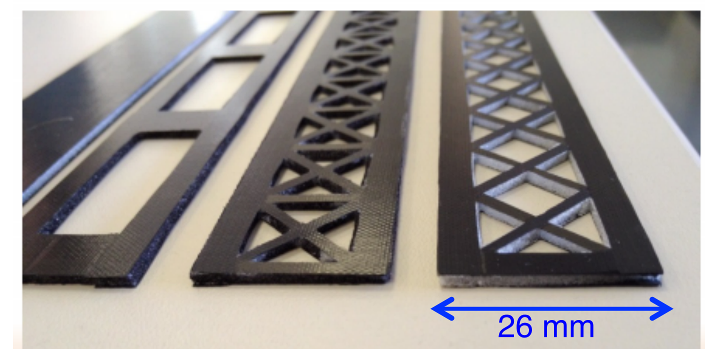




CFRP support prototypes



X/X0					
0,156 %	0,134 %	0,091 %	0,118 %	0,106 %	0,058 %



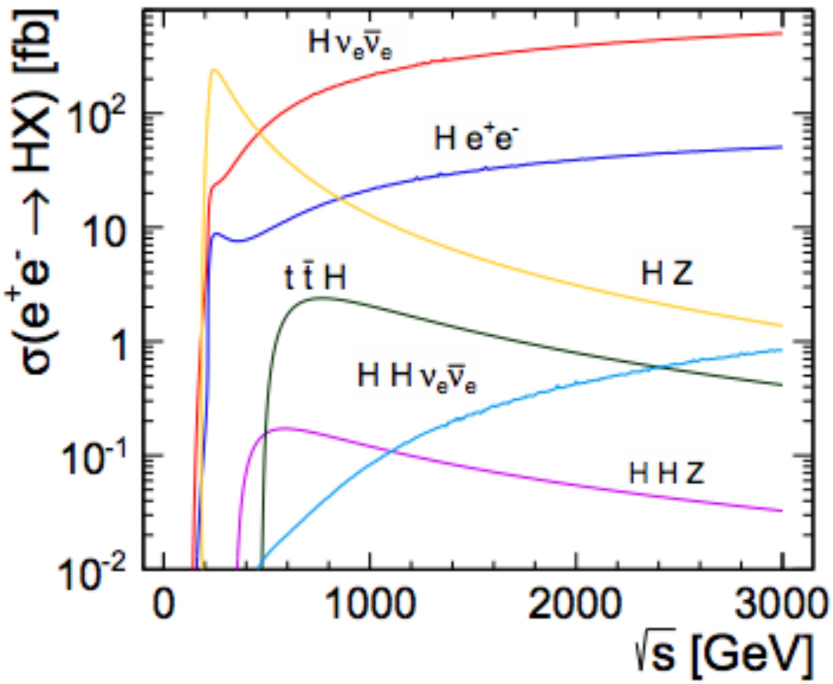
F. Nuiry, C. Bault, F. Duarte Ramos, W. Klempt

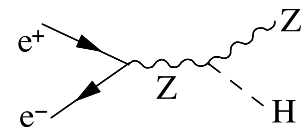
Summary and Conclusions

- CLIC accelerator provides:
  - unique potential for discovery and precision physics at the TeV scale
  - challenging requirements for vertex detectors
- Examples for active R&D on the CLIC vertex detector:
  - Hybrid pixel detector technology
  - Power-delivery and power pulsing
  - Detector cooling and mechanical integration
- Synergy between CLIC and other vertex-detector R&D projects
- Other groups most welcome to join the CLICdp studies

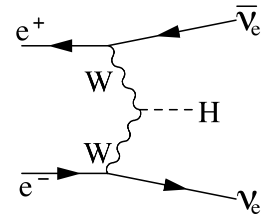
Additional material

Higgs production

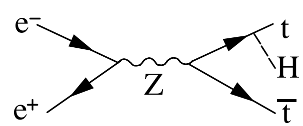




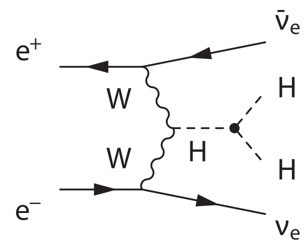
Higgs-Strahlung: $e^+e^- \rightarrow ZH$
- Measure H from Z-recoil mass
- Model-independent meas.: m_H, σ
- Measure near threshold: $\sqrt{s} \lesssim 350$ GeV



WW fusion: $e^+e^- \rightarrow H\nu_e\nu_e$
- Precise cross-section measurements in ττ, μμ, qq decay modes
- Profits from higher $\sqrt{s}$ ($\gtrsim 500$ GeV)



Radiation off top-quarks: $e^+e^- \rightarrow ttH$
- Measure top Yukawa coupling
- Needs $\sqrt{s} \gtrsim 500$ GeV



Double-Higgs prod.: $e^+e^- \rightarrow HH\nu_e\nu_e$
- Measure tri-linear self coupling
- Needs high $\sqrt{s}$ ($\gtrsim 1.5$ TeV)

Complementary Higgs measurements by accessing wide energy range:

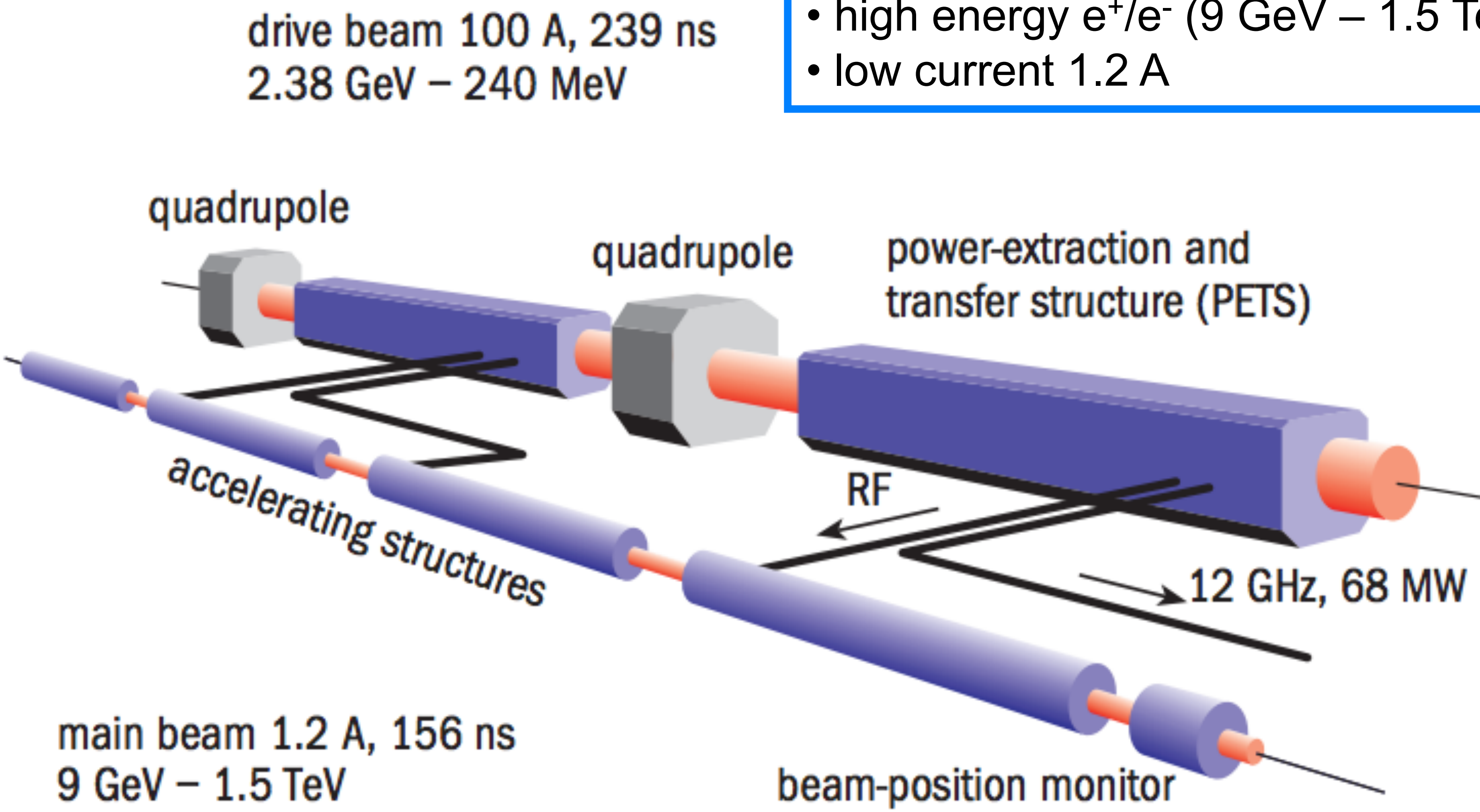
m_H=125 GeV	250 GeV	350 GeV	500 GeV	1 TeV	1.5 TeV	3 TeV
$\sigma(e^+e^- \rightarrow ZH)$	240 fb	129 fb	57 fb	13 fb	6 fb	1 fb
$\sigma(e^+e^- \rightarrow H\nu_e\bar{\nu}_e)$	8 fb	30 fb	75 fb	210 fb	309 fb	484 fb
Int. $\mathcal{L}$ (4-5 years)	250 fb^{-1}	350 fb^{-1}	500 fb^{-1}	1000 fb^{-1}	1500 fb^{-1}	2000 fb^{-1}
# ZH events	60000	45500	28500	13000	7500	2000
# $H\nu_e\bar{\nu}_e$	2000	10500	37500	210000	460000	970000

CLIC two-beam acceleration scheme

Two-beam acceleration scheme
- No individual RF power sources
- Demonstrated in dedicated test facility at CERN (CTF3)

Drive Beam supplies RF power
- 12 GHz bunch structure
- low energy e^- (2.4 GeV - 240 MeV)
- high current (100A)

Main beam for physics
- high energy e^+/e^- (9 GeV – 1.5 TeV)
- low current 1.2 A



LC pixel R&D examples

Project	Technology	Target experiments	Groups
Mimosa	**fully integrated** CMOS MAPS Tower Jazz 0.18 um	ALICE, CBM, BES-3, ILD@ILC	IPHC Strasbourg
Arachnid / Cherwell		generic vtx / tracking / calo, ALICE ITS	Bristol, Birmingham, Queen Mary, RAL, Daresbury
Chronopix	**fully integrated** CMOS MAPS IBM 90 nm	SiD@ILC	Oregon
FPCCD	**integrated sensor**, separate r/o, Hamamatsu CCDs	ILD@ILC	KEK, Tohoku
DEPFET	**integrated sensor**, separate readout, MPG-HLL DEPFET	Belle II, ILD@ILC	Bonn, MPI Munich, Barcelona, Santander, others
VIP2b / SDR / MAMBO4	**3d integrated / SOI** Tezzaron + STM 130 nm, MIT LL	generic technology tests, Super-Belle, SiD@ILC	FNAL, KEK, OKI, INFN, others
HV-CMOS CCPD	**active sensor**, 180 nm CMOS	HL-ATLAS, CLIC	Heidelberg, CERN, CPPM, Bonn, Geneva
CLICpix	**hybrid r/o**, 65 nm CMOS	CLIC, SiD@ILC	CERN

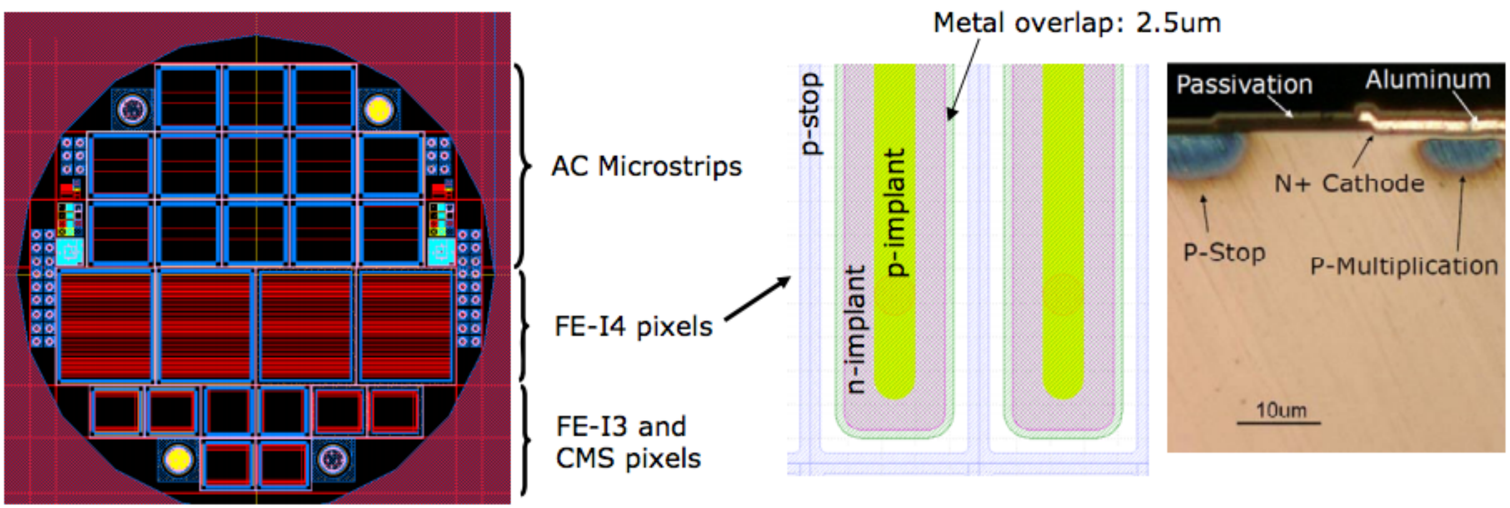
Low-Gain Avalanche Detectors (LGAD)

CLIC Detector and Physics Collaboration Meeting 01/10/2013 7

Low Gain Avalanche Detectors (LGAD)

RD50 project:
Fabrication of new p-type pixel detectors with enhanced multiplication effect in the n-type electrodes

Institutes participating in this project:
G. Pellegrini (IMB-CNM), G. Casse (Liverpool University), H. Sadrozinki (UCSC), S. Grinstein (IFAE), W. de Boer (KIT), I. Vila (IFCA), R. Bates (University Glasgow), M. Bruzzi (INFN Florence) M. Moll (CERN)



See G. Pellegrini's talk at CLIC January meeting, S. Hidalgo's talk at RD50 meeting at Albuquerque (2013) and H. Sadrozinski, "Exploring charge multiplication for fast timing with silicon sensors" 20th RD50 Workshop, Bari (2012)

cnm D. Quirion Institut de Microelectrònica de Barcelona

Low-Gain Avalanche Detectors (LGAD)

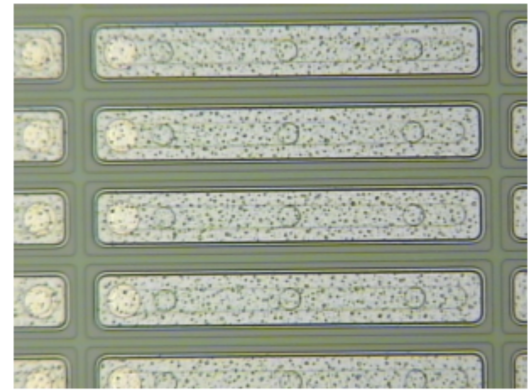
Low Gain Avalanche Detectors (LGAD): run

Substrate: Epitaxial 10, 50 & 75um / FZ HR 300um

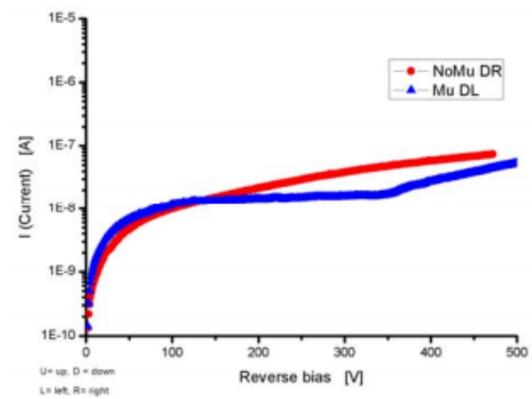
Multiplication region: With p-implant | Without p-implant

P-N junction:

- With p-implant:
  - Standard junction
  - Shallow junction
  - Deep junction
- Without p-implant:
  - Standard junction
  - Shallow junction
  - Deep junction



FE-I4 pixel sensor



AC Microstrip Epi 50um deep junction

Run finished this summer.
Sensors currently characterized at UC Santa Cruz by M. Baselga (Ph.D. student – IMB-CNM)

See G. Pellegrini's talk at CLIC January meeting and
H. Sadrozinski, "Exploring charge multiplication for fast timing with silicon sensors" 20th RD50 Workshop, Bari (2012)

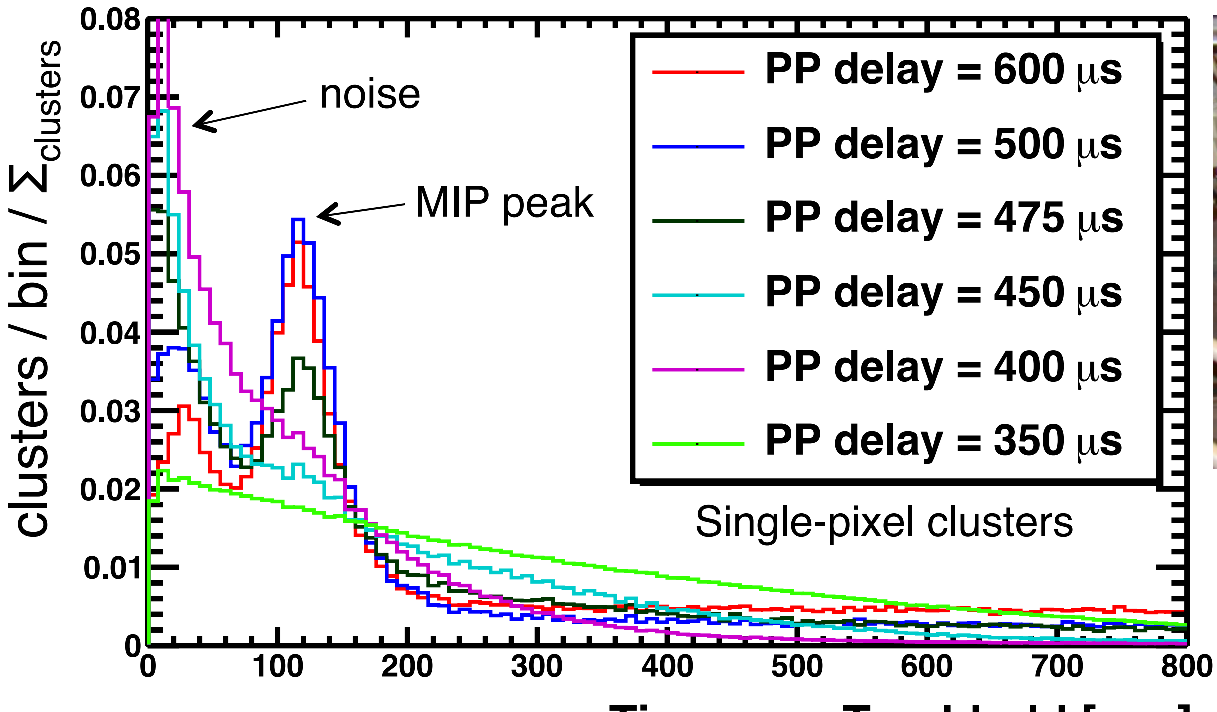
Power-pulsing in test beam

Power Pulsing with Timepix:

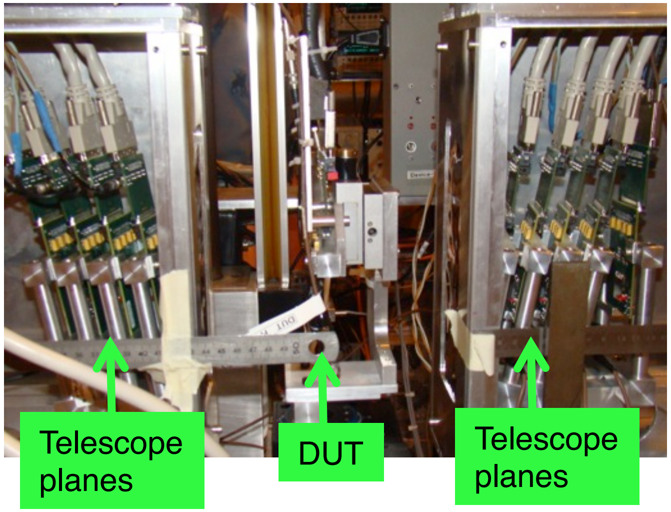
- Not designed for power pulsing, single bias line for all pixel rows
- But possibility to switch on/off all preamps through bias DAC

CERN SPS test-beam campaign in June 2012:

- Power pulsing of the Chip and operation in sync with LHCb/Timepix tracking telescope
- Shutter-based readout for 25 μs
- Adjustable delay between power-on and shutter-start times



M. Benoit



- Fully efficient after ~600 μs
- Similar results obtained with source in laboratory and in simulation